6.151 Semiconductor Devices Project Laboratory
Plans for Deep RIE and Polyimide Characterization

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During the processing of the cantilever structure, the polyimide layer performs the essential role of protecting the cantilevers during backside photoresist application, developing, deep etching and the final BOE etch. Similarly, the deep reactive ion etching process is required to anisotropically etch through the bulk of the wafer to free the cantilevers from the substrate. The goal of these experiments is to determine the proper conditions for both aspects of the overall process, and to verify that none of the other unit process steps from the Nishimoto report cause unexpected complications.

Experimental plan:

1) Control Wafer Preparation

The proposed experiments begin with the preparation of a number of wafers with oxide on one side of the same thickness as that found in the SOI wafers. These prepared wafers will permit us to examine the effects of nearly all of the processing steps on SOI substrates, without the expense of drawing upon our limited supply. At least one of the wafers will be examined using the Nanospec and color charts to verify the thickness of the oxide.

Part of the preparation of these wafers involves applying photoresist to one surface. At this time, the SOI wafers, which will eventually have test cantilevers built on them, will also be coated. While the next few steps occur, the SOI wafers will be exposed under Mask 2 to define the cantilevers, undergo RIE to etch the cantilever shape, and have the optional 250Å protective oxide grown on top. These wafers will be stored until after polyimide (PI) application has been studied. Oxide thickness will be verified by using color charts.

2) Polyimide (PI) application tests

Using these prepared wafers, and a number of fresh unaltered wafers, a series of different polyimide spin-on and bake recipes will be tested. The wafers will be optically inspected under a light microscope to check for good adhesion and uniformity in the coating.

The coated wafers will then have a 10μm thick photoresist layer applied to their back sides. These wafers will then be exposed under Mask 5 and developed. The oxide covered wafers will not undergo the photoresist development procedure until later. Inspections at this stage will include optical examination of the photoresist, and more importantly, optical examination of the polyimide to verify that the developer did not cause degradation. Thickness will be measured using the Nanospec.

Provided that the measurements are acceptable, the oxide-coated wafers will then be developed and inspected for confirmation.

3) DRIE process tests

Various recipes for DRIE will be tested using the oxide/polyimide coated wafers. These etches and corresponding inspection will likely take 2-3 lab sessions. The questions that will be answered include the following:

1. What is the profile of the sidewalls (angle, bowing, scalloping) and which recipe creates the most vertical sidewalls?
2. What is the selectivity of the etch on Si over SiO_2
3. How do the results compare with mask dimensions, and does any additional allowance need to be made?

The answers to these questions will permit us to precisely control the profile and size of the openings underneath the cantilever. They will also confirm the use of SiO_2 as an effective etch-stop material.

Measurements that are expected to be necessary include; electron microscopy to examine cross-sections of the etched wafers; and Dektak profilometry to measure any bowing of the diaphragm due to residual stresses in the oxide and polyimide. This may not be representative of the results from the SOI

wafer, but is the closest that we believe is available, barring use of actual SOI wafers. These measurements are necessary to check how much deformation the cantilever structures can be expected to endure during processing. Large bowing may plastically deform or fracture the cantilevers from their substrates.

As the DRIE processes are underway, the SOI wafers left alone during the polyimide testing will have polyimide applied according to the results of the tests in step 2, and will have photoresist applied to their backsides, exposed and developed.

4) BOE etching, ashing

The remaining oxidized control wafers will be dipped in BOE to remove the oxide and free the polyimide diaphragm. Again, optical inspection of polyimide quality will be performed, and bowing of the polyimide will be checked. Since it will be the only layer remaining, no bowing is expected.

The wafers will be ashed to remove backside photoresist and polyimide. This step is not truly necessary, but will serve to ensure that the process conditions are sufficient to clear the wafers of both materials.

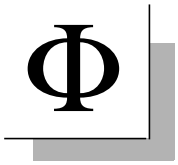
During BOE and diaphragm inspection, DRIE of the SOI wafer will be performed using the conditions determined earlier. Once complete, a BOE dip and ashing will be performed.

5) Force-Displacement tests

This step may continue into the period when the device wafers begin production. Using an AFM or other device capable of force-displacement measurements on the scale needed, these data will be acquired for the cantilevers formed on the SOI wafers to provide a look at what can be expected from the final product.

Summary

Through performing measurements on a series of test wafers, the process parameters for each step in the mechanical definition of the cantilevers can be studied. This will involve two or three plain wafers, at least eight wafers which will have oxide grown on them to simulate the buried oxide of the SOI wafers, and two SOI wafers. A variety of polyimide application recipes will be tested, as will different combinations of the DRIE parameters. Optical and mechanical measurements will provide data on polyimide thickness and adhesion, etching anisotropy and selectivity, and will reveal the effect of photoresist developer and BOE on the polyimide layer.



Fabrication Process Plan

A summary of the cleanroom processes needed to create process characterization control wafers appears in Table 1. Process step numbers and the “day number” of the lab session used to carry out the process steps, appear at the left edge of the table. A “+” appearing in the ‘day number’ column indicates that the particular procedure is conducted outside of the regular cleanroom lab session. Process step numbers within shaded blocks have cross-sectional diagrams that appear at the conclusion of this report. These diagrams are cross-sectional views of selected control wafers under construction. The right hand side of each table is populated with shaded squares in a grid. A shaded square indicates that a particular batch of control wafers (labeled with the letters of the alphabet) is subjected to the listed process step. The batch size can be a small as one wafer or as large as a dozen wafers or more.

Control wafer batches “a” and “b” begin the process as double-side polished silicon-on-insulator (SOI) wafers. Control wafer batches “p” through “x“ begin the process as plain double-side polished silicon wafers with arbitrary resistivities. Plain wafer batch “x” is used exclusively for polyimide spin-on process testing.

Table 1: Fabrication Process Summary

Day	Step	Process Operation	a	b	p	q	r	s	t	u	v	w	x
---	---	Control wafer batch “a“ and “b” consist of silicon-on-insulator (SOI) wafers: Top layer = p-type Si, 2 micron, 1 ohm-cm; Oxide layer = silicon dioxide, 1 micron; Bottom layer = p-type Si, 397 micron, 1 ohm-cm Control wafer batches “p” through “x“ are double-side polished plain silicon wafers.											
1	1	RCA wafer clean											
1	2	Wet thermal oxidation to form 1 micron oxide on both sides of plain silicon wafers											
1	3	Measure oxide thickness with Nanospec											
1	4	Verify oxide thickness with film thickness color chart											
1	5	HMDS vapor deposition (25 min. at 150 C.)											
1	6	Spin-on positive photoresist on wafer front side suitable for light RIE processing											
1	7	Photoresist pre-bake (30 min. at 90 C.)											
1	8	Mask #2 (“Cantilever definition” --- dark field) exposure											
1	9	Photoresist development, DI rinse, and blow dry											
1	10	Photoresist pattern inspection under microscope											
1	11	Photoresist post-bake (30 min. at 120 C.)											
2	12	Light RIE front side of SOI wafers to define cantilevers using multiple etching recipies if required											
2	13	HMDS vapor deposition (25 min. at 150 C.)											
2	14	Spin-on positive photoresist on wafer front side suitable for light DRIE processing											
2	15	Photoresist pre-bake (30 min. at 90 C.) and post bake (30 min. at 120 C.)											
2	16	Photoresist pattern inspection under microscope											
2	17	BOE to etch 1 micron oxide off backside of plain wafers											
2	18	Strip photoresist with Piranha etch, DI rinse, and spin dry											
2	19	Spin-on front-side polyimide using multiple recipes if required											

Table 1: Fabrication Process Summary

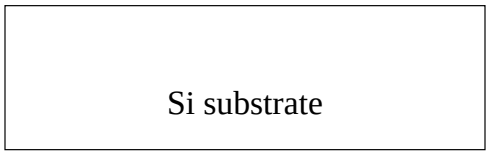
Day	Step	Process Operation	a	b	p	q	r	s	t	u	v	w	x
2	20	Cure polyimide in place											
2	21	Measure polyimide film thickness using Nanospec or other measuing instrument											
3	22	RCA wafer clean											
3	23	HMDS vapor deposition (25 min. at 150 C.) for wafer front side											
3	24	Apply protective positive photoresist to front side of wafer on top of existing polyimide layer; This layer will protect the polyimide from possible degradation by subsequent photoresist development steps											
3	25	Photoresist pre-bake (30 min. at 90 C.)and photoresist post-bake (30 min. at 120 C.) in hard bake session											
3	26	Spin-on positive photoresist suitable for extensive DRIE processing onto backside of wafers											
3	27	Photoresist pre-bake (30 min. at 90 C.)											
3	28	Mask #5 (“Backside etch” --- dark field) exposure											
3	29	Photoresist development, DI rinse, and blow dry											
3	30	Photoresist pattern inspection under microscope											
3	31	Photoresist post-bake (30 min. at 120 C.)											
4	32	RCA wafer clean											
4	33	HMDS vapor deposition (25 min. at 150 C.)											
4	34	Spin-on front-side polyimide using multiple recipes if required											
4	35	Cure polyimide in place											
4	36	Measure polyimide film thickness using Nanospec or other measuing instrument											
4	37	Apply protective positive photoresist to front side of wafer on top of existing polyimide layer; This layer will protect the polyimide from possible degradation by subsequent photoresist development steps											
4	38	Photoresist pre-bake (30 min. at 90 C.)and photoresist post-bake (30 min. at 120 C.) in hard bake session											
4	39	Spin-on positive photoresist suitable for extensive DRIE processing onto backside of wafers											
4	40	Photoresist pre-bake (30 min. at 90 C.)											

Table 1: Fabrication Process Summary

Day	Step	Process Operation	a	b	p	q	r	s	t	u	v	w	x
4	41	Mask #5 (“Backside etch” --- dark field) exposure	■	■									
4	42	Photoresist development, DI rinse, and blow dry	■	■									
4	43	Photoresist pattern inspection under microscope	■	■									
4	44	Photoresist post-bake (30 min. at 120 C.)	■	■									
4,5, 6	45	Deep reactive ion etch backside bulk silicon until etch reaches oxide etch stop layer			■	■	■	■	■	■	■	■	
+	46	Take SEM photos of control wafer cross-sections (this is a destructive test)				■		■		■		■	
7	47	Deep reactive ion etch backside bulk silicon of the SOI wafers until etch reaches oxide etch stop layer	■	■									
8	48	BOE etch through the backside oxide layer	■	■	■				■				
8	49	DI rinse and spin dry	■	■	■				■				
8	50	Ash (strip) photoresist backside and polyimide front side(and perhaps even photoresist on the front side) with oxygen plasma	■	■									
+	51	Test mechanical deflection and bowing profile of photoresist/polyimide/oxide tri-layer diaphragms with AFM or DEKTAK (assume this test is destructive)					■						
+	52	Test mechanical deflection and bowing profile of polyimide/oxide bi-layer diaphragms with AFM or DEKTAK (assume this test is destructive)									■		
+	53	Test mechanical deflection and bowing profile of photoresist/polyimide bi-layer diaphragms with AFM or DEKTAK (assme this test is destructive)			■								
+	54	Test mechanical deflection and bowing profile of polyimide single layer diaphragms with AFM or DEKTAK (assme this test is destructive)							■				
+	55	Test mechanical characteristics of cantilevers	■	■									
+	56	Prepare samples for SEM visualization of cantilever geometries	■	■									
+	57	Take SEM photos of control wafer cross-sections	■	■									

Cross-sectional diagrams through plain and SOI wafers

Plain Wafer

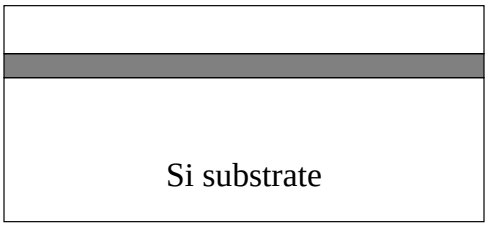


Lab Session 0

Original Wafers

SiO2

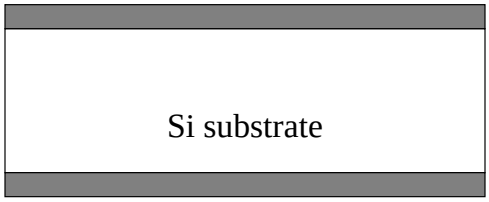
SOI Wafer



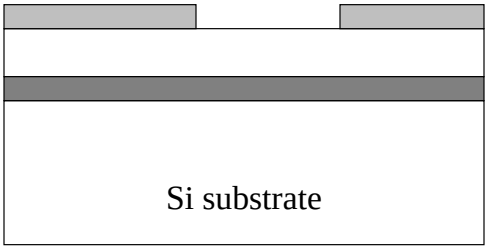
End of Lab Session 1

Steps 1-11

Photoresist



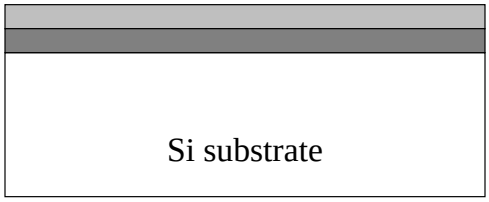
Wet thermal oxidation (1um)
Measurement of oxide thickness



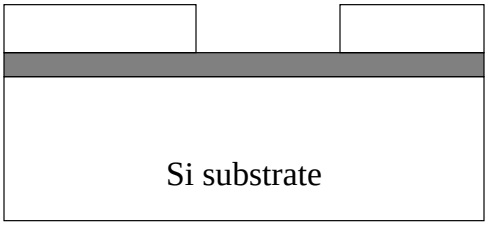
HMDS application
Front side photo, mask 2
Develop, inspect and post-bake

Lab Session 2

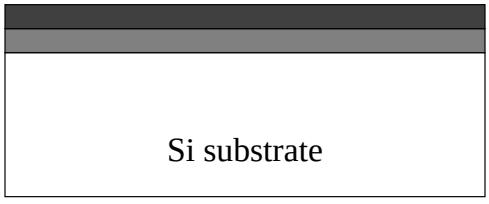
Polyimide



Steps 13-17
HMDS application
Coat front side with photoresist
BOE to remove back side oxide



Steps 12 and 18
RIE etch to define cantilever
Strip photoresist



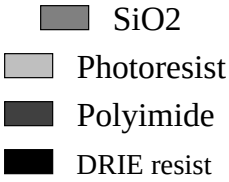
Steps 18-21
Strip photoresist
Apply and cure polyimide
Measurement of polyimide thickness

Cross-sectional diagrams through plain and SOI wafers

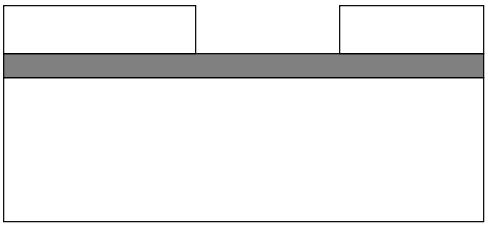
Plain Wafer

Steps 22-31
HMDS application
Apply OPTIONAL protective photoresist
Spin on and expose backside photo

Lab Session 3

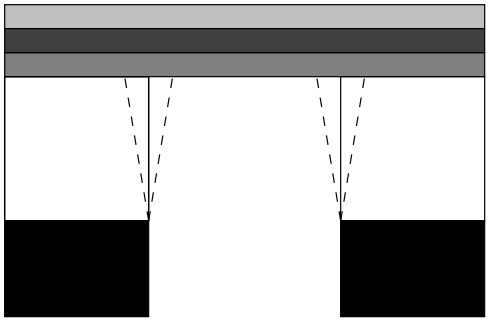


SOI Wafer

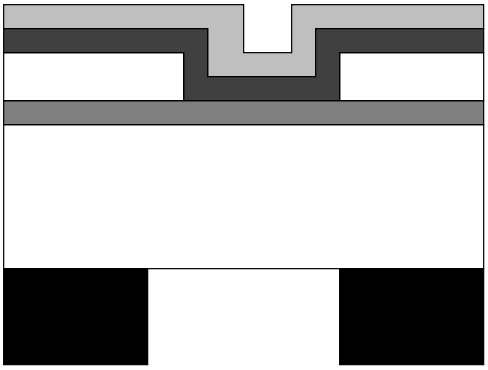


No Change

Lab Session 4-6

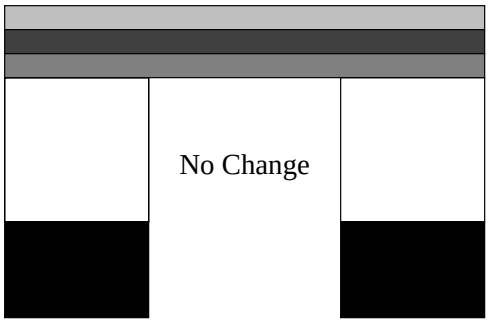


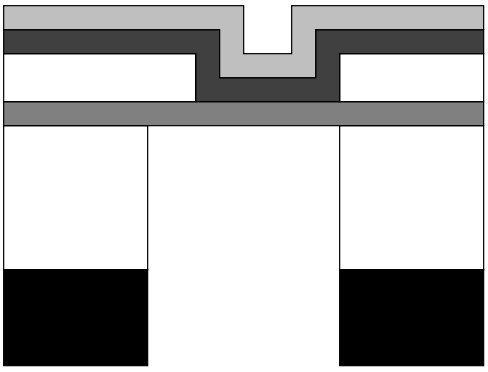
Step 45, 46
Deep RIE recipe testing
SEM imaging



Steps 32-44
HMDS application
Spin on polyimide coating
Apply OPTIONAL protective photoresist
Spin on and expose backside photo

Lab Session 7

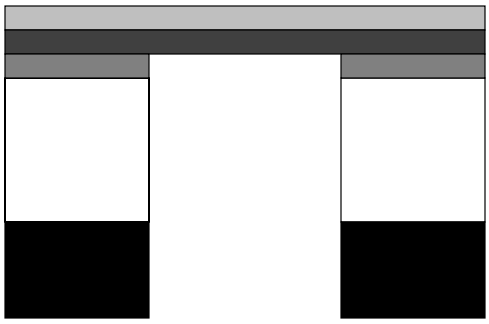




Step 47
Deep RIE of SOI wafer

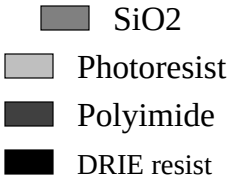
Cross-sectional diagrams through plain and SOI wafers

Plain Wafer

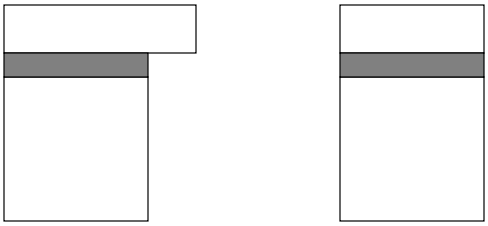


Steps 48 & 49
BOE removal of SOI oxide, rinse, dry

Lab Session 8



SOI Wafer



Steps 48-50
BOE removal of SOI oxide, rinse, dry
Ash all photoresist and polyimide

Lab Sessions 9 & 10

Steps 51-54
Measure profile of oxide/PI/photo tri-layer
Measure profile of PI/photo bi-layer
Measure profile of PI mono-layer

Steps 55-57
Test force-displacement profile of cantilevers
SEM imaging of cantilevers