Curriculum Vitae

Stephen W. Keckler

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Education:

Massachusetts Institute of Technology	PhD	Computer Science	expected 1996
Massachusetts Institute of Technology	MS	Computer Science	1992
Stanford University	BS	Electrical Engineering	1990

Experience:

Massachusetts Institute of Technology, Research Assistant *9/90-Present.*
My research focuses on the mechanisms that can be implemented in a microprocessor to enable it to serve as a node in a massively parallel fine-grained computer. My Master's thesis work proposed compile time and runtime scheduling techniques, collectively called Processor Coupling, which can be used to exploit instruction level parallelism and increase utilization of critical processor resources. To that end I wrote a processor simulator and an instruction scheduling compiler that help to demonstrate the advantages of Processor Coupling over other processor architectures. Currently, I am the lead student on the M-Machine project, an effort to build a massively parallel computer using 1995 technology. I am responsible for the processor core and am investigating how the hardware components of Processor Coupling may be implemented in VLSI. In addition I am collaborating with three other graduate students and two research staff members in the design of the memory system, network interface, and low level software tools.

Intel Corporation, Santa Clara, CA, Circuit Design Engineer, *6/89-12/89, 4/90-8/90.*
At Intel, I worked as a circuit designer on the 386SL microprocessor, under Steve Smith. My primary responsibility was to redesign dynamic CMOS programmable logic arrays to make them static. I also identified and sped up critical paths, and developed tools to integrate all of the schematics for full chip verification. My duties included specification of schematic and layout changes, supervision of changes made by layout designers, circuit simulation, functionality verification, and performance verification.

Ford Motor Company, Dearborn, MI, Systems Engineer, *6/88-9/88.*
At Ford, I designed and built an automated test system for evaluation of the ride control module used in the Lincoln Continental. In addition to checking for functionality, the system I developed also checks the margins of the diagnostic pulsewidths produced by the module.

Research Interests:

Parallel Computer Architectures: Parallel computers can employ a small set of universal mechanisms, for communication, naming, and synchronization, to exploit fine-grained concurrency. By selecting simple mechanisms that can be integrated into a VLSI processor implementation, programming systems for these computers can provide a variety of programming models and abstractions that run efficiently. These mechanisms are a fundamental part of the processor and are difficult to tack on to conventional microprocessors.

VLSI Architecture: Increased chip area and diminishing line widths provide an opportunity to integrate multiple ALUs and memory onto a single device. The resulting low interaction latency between on-chip components allows processors to employ new methods of exploiting fine grained parallelism.

Applications: Experiments in computer architecture must be application driven. By understanding the communication and synchronization requirements of real programs, such as scientific code, better architectural design decisions can be made. In addition, the mechanisms provided in the architecture can be fed back to the application designer to develop more efficient code.

Compiler Technology: With multiple ALUs on a single chip and low interaction latency between them, compile time instruction scheduling for instruction level parallelism becomes increasingly important. In addition, the compilation tools must be able to automatically map a program written for a particular programming paradigm into code that takes advantage of the set of universal mechanisms implemented in hardware.

Honors:
National Defense Science and Engineering Graduate Fellow, 1990.
National Science Foundation Graduate Fellowship winner, 1990.
Phi Beta Kappa, Stanford University, 1989.
Institute of Nuclear Power Operations Scholarship winner, 1986.
National Merit Scholarship winner, 1986.
Eagle Scout.

Memberships:
Tau Beta Pi, Sigma Xi, IEEE, ACM.

Personal:
United States citizen.
Hobbies: sailboat racing, skiing, hockey, tennis, and backpacking.

Publications:

Conference Papers:

- Stephen W. Keckler and William J. Dally, "Processor Coupling: Integrating Compile Time and Runtime Scheduling for Parallelism," *19th Annual International Symposium on Computer Architecture*, IEEE Computer Society Press, 1992, pp. 202-213.
- Nicholas P. Carter, Stephen W. Keckler, and William J. Dally, "Hardware Support for Fast Capability-based Addressing," *6th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS VI)*, 1994, pp. 319-327.

Articles:

- Stephen W. Keckler and William J. Dally, "International Symposium on Computer Architecture 1992," *Scientific Information Bulletin*, Office of Naval Research Asian Office, Vol. 17, No. 4, 1992.

Technical Reports:

- Stephen W. Keckler, *A Coupled Multi-ALU Processing Node for a Highly Parallel Computer*, MS Thesis, Artificial Intelligence Laboratory Technical Report 1355, Massachusetts Institute of Technology, 1992.

- Stephen W. Keckler, *PCS: Processor Coupling Simulator*, Concurrent VLSI Architecture Memo 42, Massachusetts Institute of Technology, Artificial Intelligence Laboratory, 1992.
- William J. Dally, Stephen W. Keckler, Nick Carter, Andrew Chang, Marco Fillo, and Whay S. Lee, *M-Machine Architecture v1.0*, Concurrent VLSI Architecture Memo 58, Massachusetts Institute of Technology, Artificial Intelligence Laboratory, 1993.
- William J. Dally, Stephen W. Keckler, Nick Carter, Andrew Chang, Marco Fillo, and Whay S. Lee, *The MAP Instruction Set Reference Manual v1.0*, Concurrent VLSI Architecture Memo 59, Massachusetts Institute of Technology, Artificial Intelligence Laboratory, 1993.
- William J. Dally, Stephen W. Keckler, Nick Carter, Andrew Chang, Marco Fillo, and Whay S. Lee, *M-Machine Microarchitecture v1.0*, Concurrent VLSI Architecture Memo 60, Massachusetts Institute of Technology, Artificial Intelligence Laboratory, 1993.

Recent Presentations:

- *The M-Machine Multicomputer*, presented at Princeton University, Princeton, NJ, June 3, 1994.
- *Processor Coupling: Integrating Compile Time and Runtime Scheduling for Parallelism*, presented at the 19th Annual International Symposium on Computer Architecture, Gold Coast, Queensland, Australia, May 20, 1992.
- *Processor Coupling*, presented at the NATO Advanced Study Institute "Parallel Computing on Distributed Memory Multiprocessors," Ankara, Turkey, July 10, 1991.