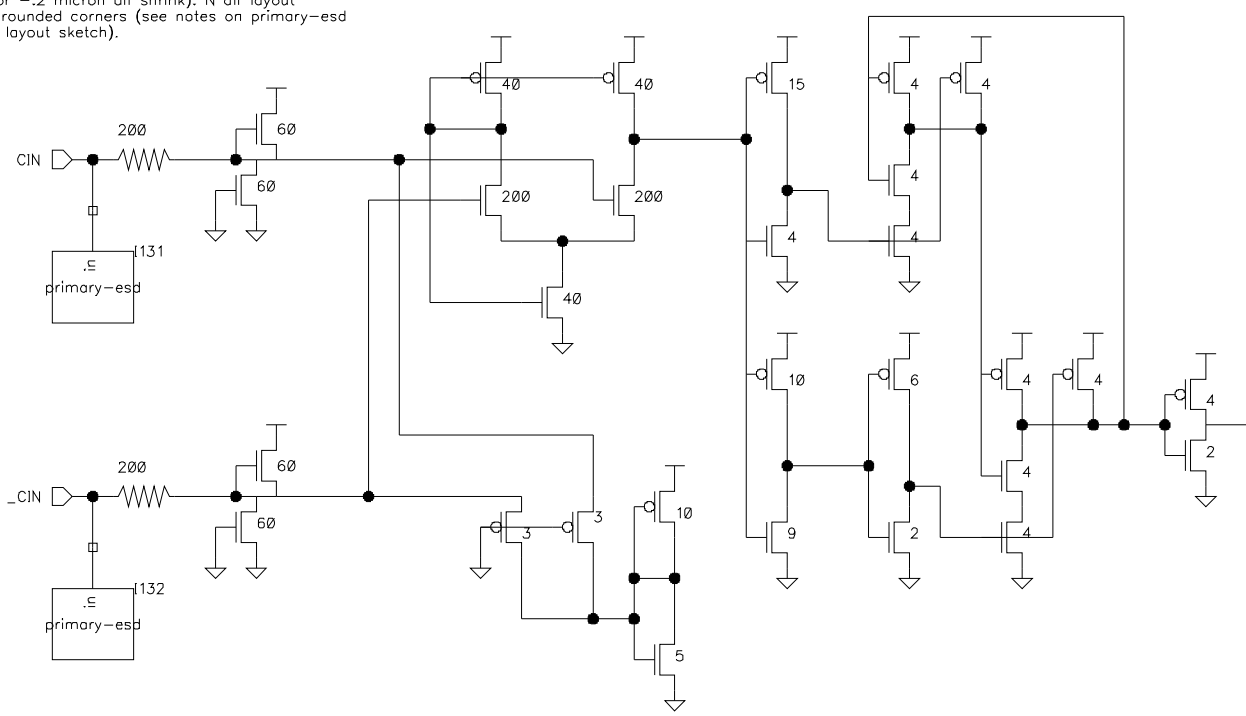
CAGE NO.	DWG NO. tk2/input-c

Note: All transistors shall be aligned in a single geometric orientation on the die. Differential pairs shall be aligned such that current flows through transistors in the same physical direction in each branch.

Note: all power and ground wires shown on this page shall be tied together and connected to other power/ground wiring through a single metal wire path each. (No external current flow through cell pwr/gnd).

Note: 200 ohm resistor is fabricated as 67 squares (200 microns) of 3.2 micron wide N diffusion over substrate. (3.2 micron rather than 3 microns to account for −.2 micron dif shrink). N dif layout must use rounded corners (see notes on primary−esd sheet and layout sketch).

Note: Primary ESD protection and diffusion resistor in the input protection network shall be surrounded completely by a guard ring consisting of a minimum of 30 microns wide N−well, with N−diffusion interior to the well (well contact). Contacts are made to the N−dif in the well as frequently as possible to metal−1. The metal−1is connected to Vdd. The N−well guard ring is surrounded entirely by a minimum width of 30 microns of P−diffusion in the substrate (substrate contact). P−dif is contacted as frequently as possible to metal−1, which is tied to ground.



Polych
Input

DRAWN BY	DATE
Tom Knight	Nov 15 19:1