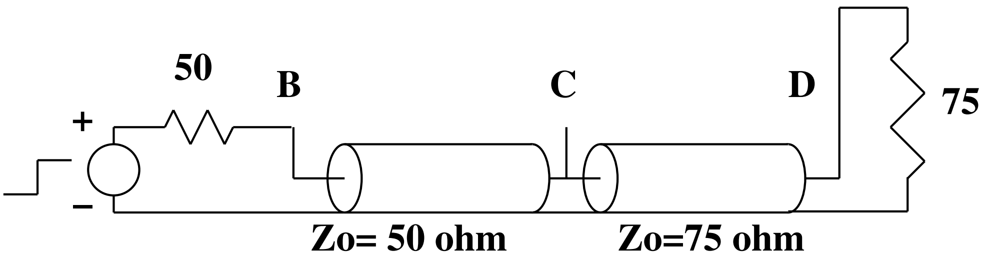
Massachusetts Institute of Technology

Department of Electrical Engineering and Computer Science

6.313 Contemporary Computer Design

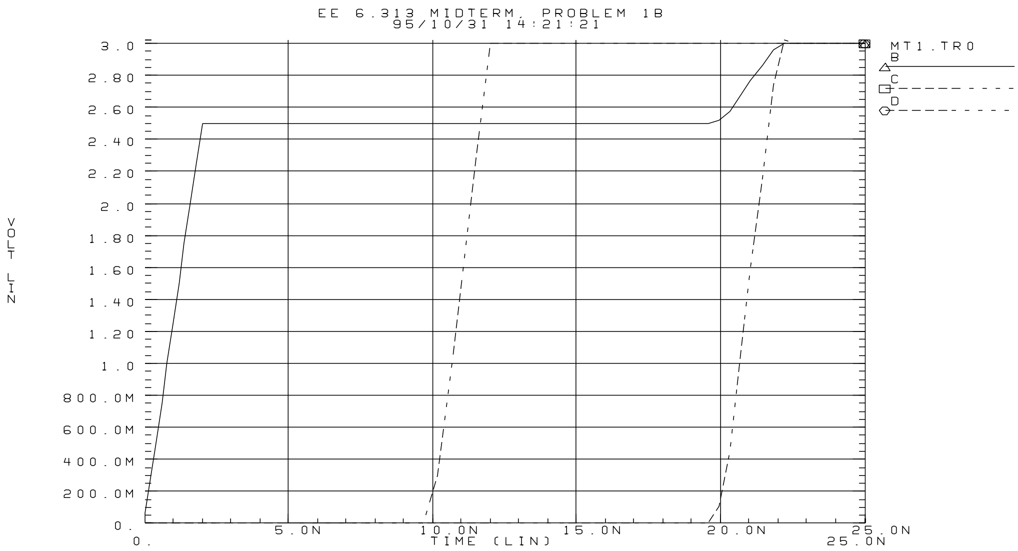
Midterm Exam Solutions, November 1, 1995

1. (35 pts) Figure 1 shows the thevenin equivalent model of the driving gate, transmission line segments, and termination:



a) At point (C), the line appears to be a 50Ω line terminated by a 75Ω resistor, since the75Ω line is properly terminated. The reflection coefficient $\Gamma = \frac{75-50}{75+50} = \frac{1}{5}$.

b) c) d)



e)

$$w = \frac{h}{Z_0}\sqrt{\frac{M}{K}}\sqrt{\frac{\mu_0}{\epsilon_0}} = \frac{1mm}{50\Omega}\sqrt{\frac{1}{4}}377\Omega = 3.77mm \quad (1)$$

f)

$$l = t \times v = 10ns \times \frac{c}{\sqrt{MK}} = 1.5m \quad (2)$$

g)

$$w = \frac{h}{Z_0}\sqrt{\frac{M}{K}}\sqrt{\frac{\mu_0}{\epsilon_0}} = \frac{1mm}{75\Omega}\sqrt{\frac{1}{4}}377\Omega = 2.51mm \quad (3)$$

h) Again the length is 1.5m. The speed of the wave only depends on the material properties M and K.

2. (30 pts) $15mm \times 19mm = 285mm^2$

a) $2\% \times 285mm^2 = 5.7mm^2$
$C = K\epsilon_0 \times Area/t = 3.9\epsilon_0 \times 5.7mm^2/10nm = 19.7nF$

If you modified the width of the gates to account for peripheral (fringing) capacitance, the area becomes $(w+\frac{3}{4}h)\times l$. Making some reasonable assumptions about the number of transistors and the relationship between the width and length, the modified area becomes $5.710mm^2$, and the original area is $5.700mm^2$. Clearly fringing fields are relatively unimportant in this case.

b) $C = K\epsilon_0 \times Area/t = 3.9\epsilon_0 228mm^2/1\mu m = 7.87nF$

c) $E = 20\% C_{total}V^2 = 20\%(C_{gate} + C_{wire}) \times 3.3^2 = (20\% 27.57nF)3.3^2 = 60.0nJ$

d) If we assume that the power dissipated by the processor in an average cycle is totally due to switching 20% of the gate and wire capacitance,
$P = 20\% C_{total}V^2 f = 20\%(C_{gate} + C_{wire}) \times 3.3^2 \times 100MHz = 6W$

e) The energy available from the battery is $E = 10A \times 7.5V \times 1hour = 75Whr = 75W \times 3600s = 270kJ$. With a 90% power conversion efficiency, 67.5 W hr (or 243kJ) are available to the laptop. The system is consuming 6W + 8.4W = 14.4W. The power consumed times the battery lifetime equals the energy available from the battery, or $14.4W \times t = 67.5Whr = 243kJ \Rightarrow t = 4.7hours(or 16,875s)$

e) $i = 5\% C\frac{dV}{dT} = 5\% 27.57nF\frac{3.3}{100ps} = 45.5A$

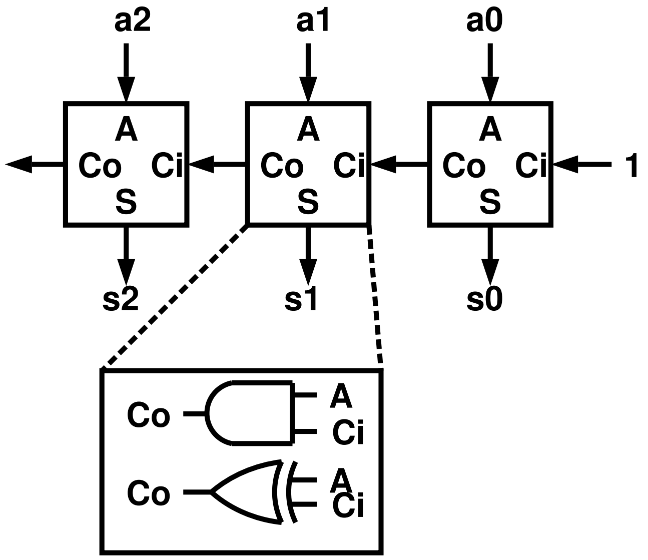
f) $di/dt = 45.5A/100ps = 455 \times 10^9 V/H$

f) ** Bonus Question **

3. (35 pts)

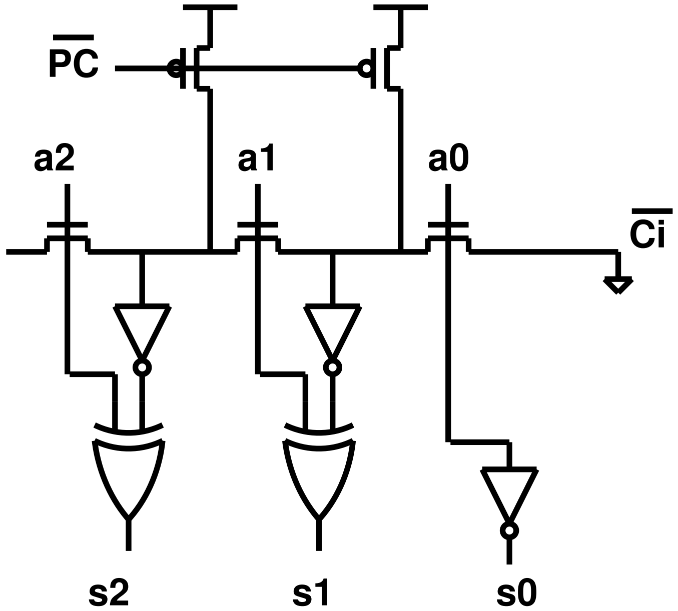
a) $S = A \oplus C_i$
$C_o = A \cdot C_i$

A_i	C_i	S	C_o
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



b) Delay scales linearly with N.

c) The Manchester carry chain in the case of an incrementer does not have a generate or kill signal, and the propagate value is simply the value of the A input.



d) For a long chain, the carry chain looks like a distributed RC line with delay scaling with L^2, or N^2. Since the chain does not have a kill signal, no modifications are necessary when using inverters (rather than non-inverting buffers) to periodically buffer the signal along the line. The designer must only ensure that the polarity of the carry bits being used along the line are respected (but the chain itself does not need modification).

e) $C_{o_4} = A_3(A_2(A_1(A_0)))$

f) In a noisy environment, precharged logic is inappropriate, so either standard static CMOS or carry lookahead are suitable. With a very fast NOR gate, carry lookahead, with its requirement for a high fan-in AND gate, is very appropriate. Simply invert the inputs and by DeMorgan's theorem, the NOR becomes an AND. And for minimal area, the two transistor Manchester carry chain stage is very attractive.