Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.313 Contemporary Computer Design

Problem Set #3 Sept 27, 1995, Due Wed 4 October

PS #2 Corrections:
2 (d) All the capacitors are in parallel, so the total $C = 6 \times (4.4pF + 8pF) + 36pF = 110.4pF$ so $\mathcal{C} = 110.4pF/30cm = 368pF/m$
2 (f) $v = \frac{1}{\sqrt{\mathcal{LC}}} = \frac{l}{\sqrt{LC}} = c/3.15$

1. a) $MPZPZ = -11010 = -1 \times 3^4 + 1 \times 3^3 + 1 \times 3^1 = -51$
It is unique.

b)

Cin	A	B	Cout	Sum
M	M	M	M	Z
M	M	Z	M	P
M	M	P	Z	P
M	Z	M	M	P
M	Z	Z	Z	M
M	Z	P	Z	Z
M	P	M	Z	M
M	P	Z	Z	Z
M	P	P	Z	P
Z	M	M	M	P
Z	M	Z	Z	M
Z	M	P	Z	Z
Z	Z	M	Z	M
Z	Z	Z	Z	Z
Z	Z	P	Z	P
Z	P	M	Z	Z
Z	P	Z	Z	P
Z	P	P	P	M
P	M	M	Z	M
P	M	Z	Z	Z
P	M	P	Z	P
P	Z	M	Z	Z
P	Z	Z	Z	P
P	Z	P	P	M
P	P	M	Z	P
P	P	Z	P	M
P	P	P	P	Z

c) In a sum of products binary arrangement, each AND gate detects a particular input condition and fires. The OR gate reports success of any AND detector. This is universal because any particular input condition can be detected by an AND gate with inverters on the appropriate inputs, and the result of that detection can

be either high or low regardless of the conditions of the other detectors, so any input condition can produce any output condition. Since the AND/OR structure can be built with only NAND or NOR gates, these gates are universal.
In ternary logic, we want a similar structure: a series of detectors which trigger a MAX gate. The inputs of the detectors (we only need a detector which signals a 1 for all inputs = 1 and -1 otherwise, and a detector which signals a 0 for all inputs = 1 and -1 otherwise) must be setable to 1, so we need 3 gates which select out M, Z, and P and set the value of interest to 1 and the other two values to -1. We now have 6 gates (MAX, two detectors, and 3 selector gates). To reduce this number, we note that this function, which we call foo:

		B		
		M	Z	P
	M	P	P	P
A	Z	P	P	Z
	P	P	Z	M

can implement the 3 selector gates (eg select 1 is the inverse of foo with both inputs tied together, so $-1 \rightarrow -1, 0 \rightarrow -1, \rightarrow 1$) and both detector gates. So all we need is MAX and foo. It is also apparently possible to implement MAX with foo.

d) Looking at the two input addition table and ignoring symmetric entries (eg A=1 B=0 is the same as A=0 B=1) we have:

A	B	Cout	Sum
-1	-1	-1	1
-1	0	0	-1
-1	1	0	0
0	1	0	1
0	0	0	0
1	1	1	-1

This is a ternary half adder. Connecting two half adders and a sum block creates a full ternary adder. These full adders are then connected in a ripple chain to create a ripple adder. The third block is a sum because the two carries from the half adders are never greater than 1, so there is no carry from the sum.

e) For $-2V < V_{in} < -2/3V$, $V_{out} = 2V$.
For $-2/3V < V_{in} < 2/3V$, $V_{out} = 0V$.
For $2/3V < V_{in} < 2V$, $V_{out} = -2V$.

f) The Fnordian inverter resembles a standard binary inverter, with a PMOS transistor tied to +2V, the input, and the output, and an NMOS transistor tied to the output, input, and -2V. The additional component is a (ratioed) resistor between the output and 0V.

g) A simple CMOS NAND with the output resistively connected to ground will implement 8 of the 9 output values, but for a ZZ input, it will give a Z output instead of the desired P. A transistor with a lower V_t will allow us to detect the case of ZZ input and bring the output high.

2. a) $t_d = n(\mathcal{RC}(\frac{L}{n})^2) + Tn = \mathcal{RC}\frac{L^2}{n} + Tn$

b) $\frac{d}{dn}(a) = -\mathcal{RC}\frac{L^2}{n^2} + T \Rightarrow n = \sqrt{\frac{\mathcal{RC}L^2}{T}}$

c)

$$\begin{aligned} t_d &= \mathcal{RC}\frac{L^2}{n} + Tn \\ &= \mathcal{RC}L^2\sqrt{\frac{T}{\mathcal{RC}L^2}} + T\sqrt{\frac{\mathcal{RC}L^2}{T}} \\ &= \sqrt{\mathcal{RC}L^2T} + \sqrt{\mathcal{RC}L^2T} \\ &= 2L\sqrt{\mathcal{RC}T} \end{aligned}$$

The time taken in the interconnect is half the total time taken in the wire.

d) $\mathcal{RC}L^2$ is constant under scaling, and if T decreases with scaling, n will increase as we scale and the total delay will decrease slightly (as the square root of T) with scaling.

3. a)

b) The inverter does not regenerate logic signals which drop below their maximum levels. The gate therefore can not be combined with other gates in a logic family.

c) Quite a few solutions exist. A ring oscillator composed of these devices would quite quickly cease functioning.