CURRICULUM VITAE

Thucydides Xanthopoulos

Work Address
50 Vassar Str., Room 38-107
Cambridge, MA 02139
TEL (617) 258-8102
FAX (617) 253-5053
E-mail: duke@mtl.mit.edu

Home Address
540 Memorial Dr., Apt. 703
Cambridge, MA 02139
TEL (617) 621-1685

Areas of Interest

Low power digital VLSI design, CAD tool development for ASIC design, multimedia applications, parallel processing, high performance computer architecure.

Education

Massachusetts Institute of Technology **1988---present**
Candidate for a Ph.D in Electrical Engineering and Computer Science.
Research Areas: Low power video decompression, computer-aided modelling of power dissipation in digital systems.
Relevant coursework: Digital and analog VLSI design, computer-aided design, semiconductor device physics, signal processing, computer architecture, stochastic processes and estimation, parallel processing.

Master of Science in Electrical Engineering and Computer Science, February 1995.
GPA 5.0/5.0

Bachelor of Science in Electrical Engineering, June 1992
GPA: 4.9/5.0

Academic Honors

Massachusetts Institute of Technology **1988---present**
Vice President HKN BΘ Chapter 1991-1992
Member HKN, ΤΒΠ 1991---present
Recipient of the IEEE Boston Chapter Power Engineering Society Award for Academic Excellence, June 1991.
Received letters of commendation for outstanding performance in three undergraduate courses in the EECS Department (Circuits and Electronics, Digital Systems Laboratory, Devices and Circuits.)

Experience

MIT Microsystems Technologies Laboratories **1995---present**
Currently designing a low power MPEG-2 video decompression chip under the supervision of professor Anantha Chandrakasan, focusing on both algorithmic and circuit optimizations for reducing power dissipation. The project involves algorithmic design, RTL (Verilog) modelling, schematic design, layout, verification and testing. The prototype will be built in a state-of-the-art 0.5 um CMOS process.

Designed and tested PYTHIA 1.0, a Verilog-based power estimation software tool. PYTHIA works with a structural Verilog circuit description. It is capable of estimating circuit power dissipation by monitoring signal transitions on all circuit nets and relies on minimally annotated standard cell libraries. PYTHIA output has been compared to Hspice and Powermill output for a number of test circuits. Results have been very similar and consistent. Deviations range from 2%-30% depending on the circuit, technology and supply voltage level. PYTHIA binaries will soon be freely available to the design community over the Internet.

Co-designed and built a test chip for the new Lincoln Laboratory Silicon-on-Insulator (SOI) process. The chip includes four different arithmetic units (3 adders and 1 multiplier). It features direct back gate contacts for theshold voltage control of every transistor on the chip. The chip will test the concept of varying the treshold voltage to reduce power dissipation and facilitate operation of systems with variable supply voltages.

MIT Artificial Intelligence Laboratory **1992---1995**

Co-designed and built the Reliable Router, a 600,000-transistor 16x14 mm ASIC under the supervision of prof. Bill Dally. The Reliable Router is a network switching element used to construct reliable and high-performance tightly coupled multicomputer networks. It features novelties such as adaptive routing, multiple virtual channels, simultaneous current-mode bidirectional signalling, plesiochronous data retiming, message replication within the network and reliable error handling. Co-supervised and guided a team of undergraduate students working on various aspects of the project.

Designed a reliable adaptive routing algorithm for wormhole-routed multicomputer networks. Proved analytically freedom from deadlock and embedded this routing algorithm in the Reliable Router ASIC. Designed a graphical software package in C using Tcl/ Tk to visualize the routing algorithm and construct an additional exhaustive proof of freedom from deadlock. The package also serves as a design tool for wormhole routing algorithms.

Bolt, Beranek & Newman, Cambridge MA **Summer 1995**

Worked on the BodyLAN project which develops a wireless network of small body sensors communicating with a hand-held hub. Was responsible for the development of orthogonal codewords for CDMA communication between each sensor and the hub. Developed software for the computation of optimal Optical Orthogonal Codes (OOC) using concepts from Galois fields and finite geometries. Moreover, developed software for greedy and fast generation of codewords with parametrized auto- and cross-correlation properties.

MIT Artificial Intelligence Laboratory **1991---1992**

Designed and built a high-performance disk array for the J-Machine, a fine-grain, massively parallel computer conceived and designed by prof. Bill Dally and the Concurrent VLSI Architecture Group. Designed a PC board built around the NCR 53c90 SCSI Enhanced Processor and wrote low-level SCSI drivers for disk access. The board featured DMA and dual-ported sector buffers.

CAD Experience

Extensive experience with Cadence Design Framework II, SKILL Development, Verilog-XL including PLI programming, Chronologic VCS, Hspice, Powermill, Wattwatcher, Undertow, Signalscan, Magellan, Matlab, and public domain design tools such as Magic and IRSIM.

Developed software to port Magic standard library cells to the Cadence DFII format with retargeteable design rules.

Publications

<ins>“A Data-Diven IDCT Architecture for Low Power Video Applications”</ins> by Thucydides Xanthopoulos, Anantha P. Chandrakasan, Charles G. Sodini and William J. Dally. Submitted to the European Solid State Circuits Conference (ESSCIRC ‘96), September 1996.

<ins>“Low-Latency Plesiochronous Data Retiming”</ins> by Larry R. Dennison, William J. Dally and Thucydides Xanthopoulos. Proceedings of the 1995 Advanced Research in VLSI Conference, Chapel Hill NC, March 1995

<ins>“Fault-Tolerant Adaptive Routing in Multicomputer Networks”</ins> by Thucydides Xanthopoulos. MIT Master Thesis, February 1995.

"Architecture and Implementation of the Reliable Router" by William J. Dally, Larry R. Dennison, Kinhong Kan, David Harris and Thucydides Xanthopoulos. Proceedings of Hot Interconnects II, Stanford CA, August 1994.

"The Reliable Router: A Reliable and High-Performance Communication Substrate for Parallel Computers" by William J. Dally, Larry R. Dennison, Kinhong Kan, David Harris and Thucydides Xanthopoulos. Proceedings of the First International Parallel Computer Routing and Communication Workshop, Seattle WA, May 1994.

"A Disk Array for the J-Machine" by Thucydides Xanthopoulos. MIT Bachelor Thesis, June 1992.

Conference Presentations

First International Parellel Computer Routing and Communication Workshop, Seattle WA, May 1994.
Talk title: "The Reliable Router: A Reliable and High Performance Communication Substrate for Parallel Computers."

Supercomputing '94, Washington DC, November 1994.
Poster presentation title: "Overview of the Reliable Router."

References

Anantha P. Chandrakasan — anantha@mtl.mit.edu
MIT Professor of Electrical Engineeering — (617) 258-7619

William J. Dally — billd@ai.mit.edu
MIT Professor of Electrical Engineering and Computer Science — (617) 253-6043

Larry R. Dennison — dennison@bbn.com
BBN Senior Engineer — (617) 873-2692