Process Development and Fabrication of Piezoresistive Microcantilevers

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Introduction

Silicon processing technology has evolved into a mature industry over the last 40 years. In the last 15 years, the processing techniques developed and refined to enable large-scale integrated circuit fabrication have been modified to produce microelectromechanical systems. MEMS devices have been incorporated into many products including pressure sensors, accelerometers, and ink jet print heads. The microcantilever is a particularly useful MEMS structure. For example, a microcantilever can be used as the sense element for atomic force microscopy (AFM) and high resolution chemical analysis.

An AFM cantilever is a long thin beam of silicon with a pointed protruding tip. This tip is dragged or tapped over the surface of a sample and the deflection of the cantilever can be optically monitored with a laser beam. The deflection can also be measured in the electrical domain by observing the change in resistance of a piezoresistor imbedded into the cantilever.

Very sensitive chemical sensors can be constructed from cantilevers coated with an analyte absorbing chemical. The absorbed material causes the beam to bend, and the deflection can then be monitored as a resistance change in an imbedded piezoresistor. One advantage of microcantilever chemical sensors (MCS) is the very small size of the sensing area. This small area gives MCS devices a sensitivity that can be as high as two orders of magnitude greater than that for other chemical sensors. Also, large numbers of chemical sensing cantilevers can be fabricated from a single silicon wafer.

Over the course of 12 weeks, we developed and executed a process flow which enabled the fabrication of more than 700 piezoresistive cantilevers on an SOI silicon wafer. Fabrication processes were carried out at the MIT Microsystems Technology Laboratories. Testing of the completed devices was carried out at the MIT Media Laboratory. This report documents the fabrication, experimental design, and characterization of the mechanical and electrical properties of the cantilevers and associated test structures.

As a brief summary of the results: The piezoresistive cantilevers had a resonant frequency of 44 kHz (+/- 1 kHz), a spring constant of 1.3 N/m, a deflection sensitivity of 0.51% dR/R per micron of tip deflection, and a gage factor of at least 68. The process yield was better than 99.5%.

Fabrication Overview

Geometry, Die Layout, and Mask Set

The piezoresistive cantilevers were fabricated from an SOI wafer using a series of frontside definition and backside deep etch steps. As shown in Figure 1, each piezoresistive microcantilever was designed to be 200 microns long, 50 microns wide, and 2 microns thick. Aluminum contacts were made to either end of a looped piezoresistor that extended 90 microns from the root of the microcantilever. Total piezoresistor length was approximately 200 microns. As shown in Figure 2, eight microcantilevers were included in each die, and approximately 90 dies were fabricated on a single four inch wafer. Three of the cantilevers on each die were attached to a "snap-away" section that could be removed without the use of a die saw. The remaining five microcantilevers were attached to the bulk wafer for testing purposes. The border of the die was left intact to preserve the rigidity and structural stability of the wafer. The central area in the die was used for alignment markings. Registration tolerance of all frontside features was five microns. Backside features, which were aligned using an infrared alignment tool, had a registration tolerance of ten microns. The remaining area of the die was dedicated to test structures and electrical connections. The test structures were used measure various device parameters. Contact resistance and resistivity were measured using a Van der Paus structure. A capacitor diode was used to measure oxide thickness and junction characteristics. The capacitor diode is composed of a diffused region overlaid with oxide and metal. Contacts are made to the surrounding substrate and the diffused region below the device. The five mask set used for the photolithographic steps in the process flow is presented in Figure 3.

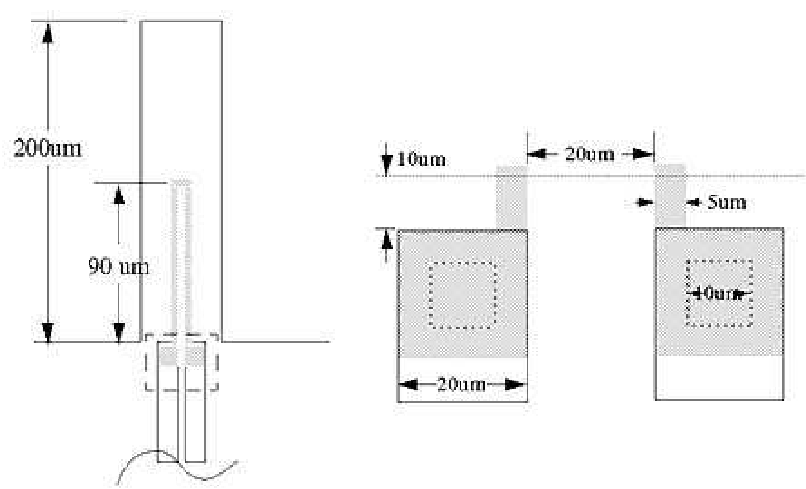


Figure 1 --- The microcantilever is 200 microns long, 50 microns wide, and 2 microns thick. The cantilever hangs out over a deep DRIE cut made into the backside of an SOI wafer. Aluminum contacts are made to either end of a looped piezoresistor that extends 90 microns from the root of the microcantilever. Total piezoresistor length in approximately 180 microns.

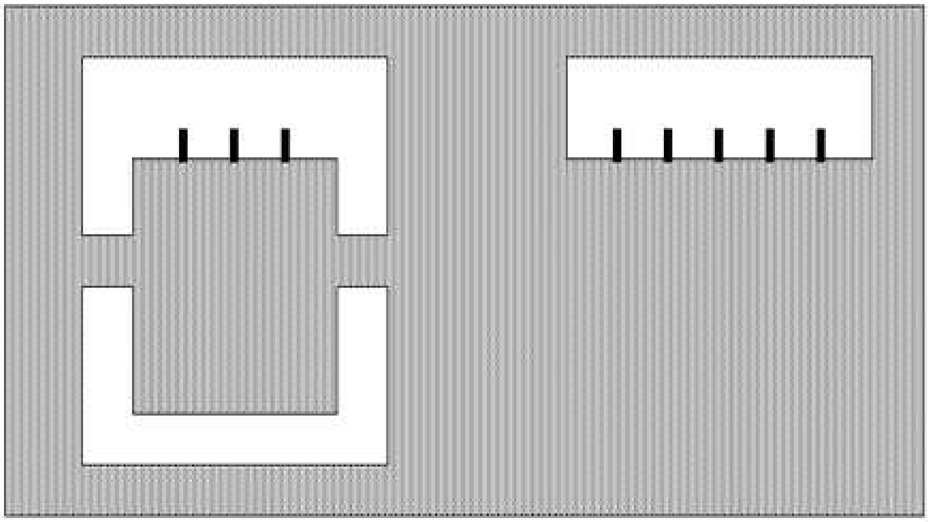


Figure 2 --- Three microcantilevers are attached to one end of a section that can be snapped out and removed from the wafer. Five additional un-releaseable microcantilevers are included on the die for testing purposes.

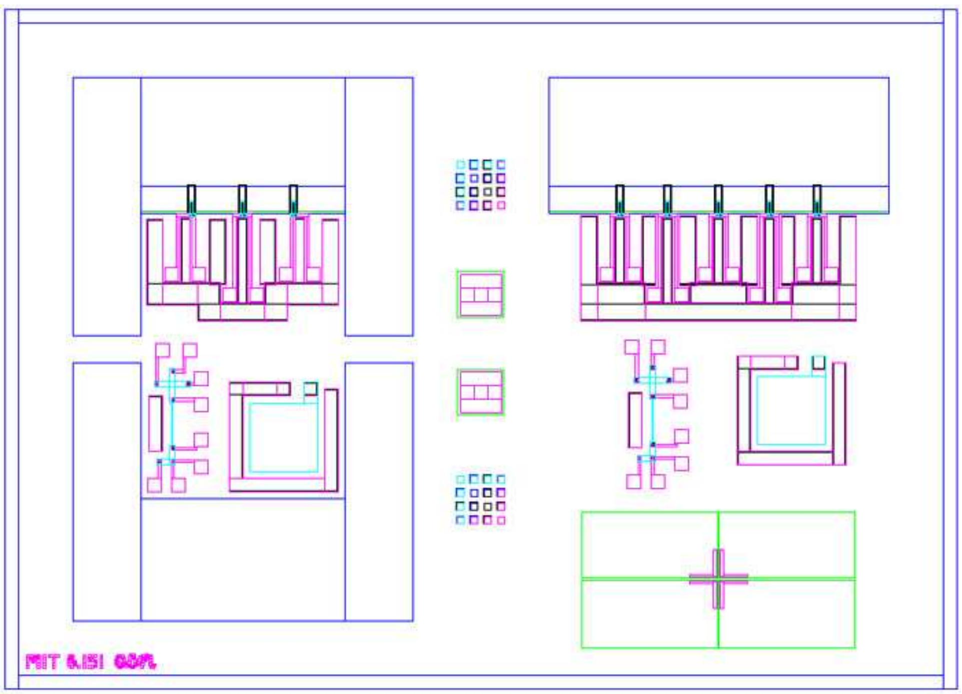


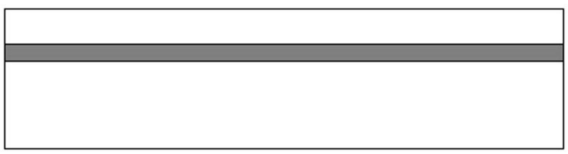
Figure 3 --- Five masks were used for the photolithographic steps in the process flow: Mask #1 ("Piezoresistor Definition Mask") --- shown here in light blue; Mask #2 ("Cantilever Definition Mask") --- shown here in ; Mask #3 ("Contact Holes Mask") --- shown here in ; Mask #4 ("Metal Definition Mask") --- shown here in magenta; Mask #5 ("Deep Etch Mask") --- shown here in dark blue.

Process Flow

The fabrication process flow is summarized in the series of cross-section diagrams that appear below. A detailed description each process step can be found in bulleted form in Appendix A.

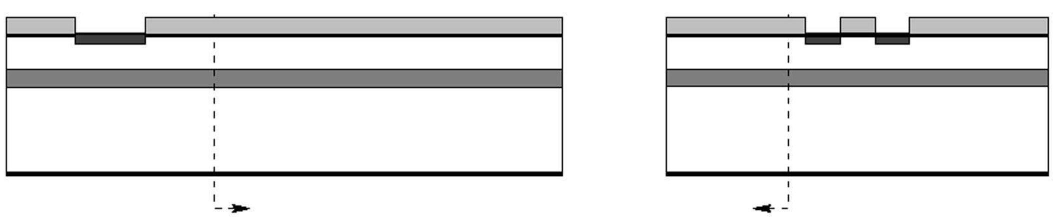
Starting Material

- Commercially prepared SOI wafer with 1 micron embedded oxide layer and 2 micron upper silicon layer



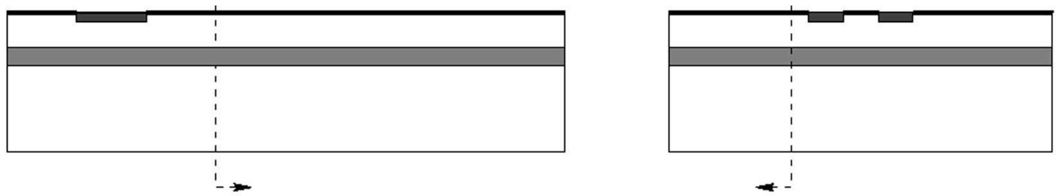
Processes 1 – 5

- RCA clean
- Grow 240Å oxide (shown with thick black line)
- Counter dope upper silicon layer with boron (5×10^{12} cm^{-2})
- Photolithography using Mask #1 ("Piezoresistor Definition Mask")
- Implant arsenic (10^{16} cm^{-2}) (shown as dark region)



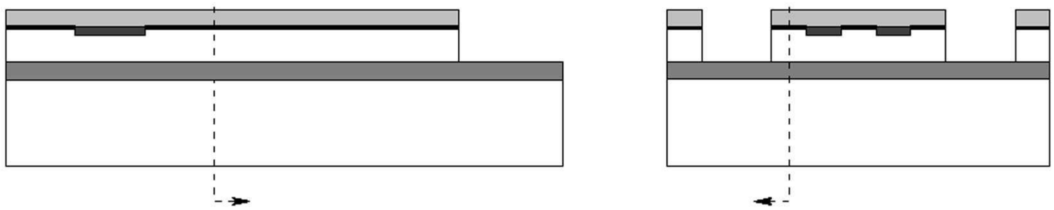
Processes 6 – 7

- BOE to remove oxide over piezoresistors
- Ash photoresist



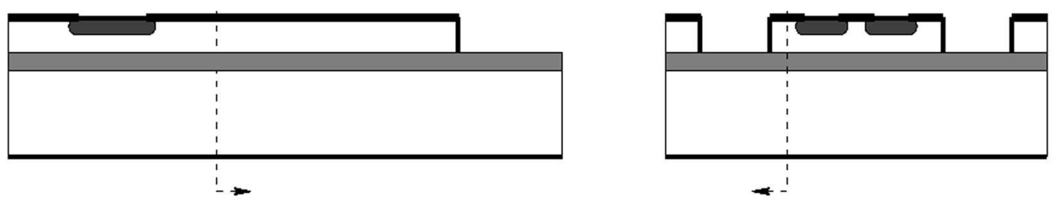
Processes 8 – 10

- Photolithography using Mask #2 (“Cantilever Definition Mask”)
- Clear oxide with BOE
- Etch out lateral dimensions of cantilever with DRIE etch



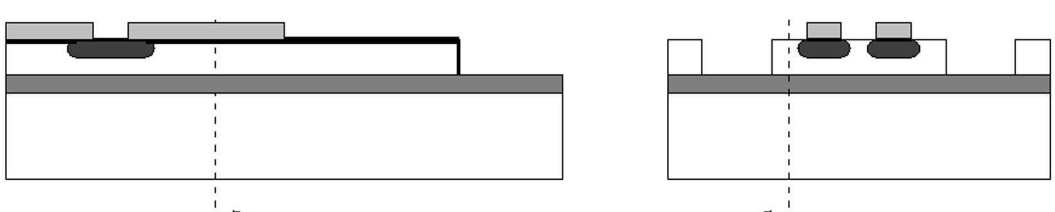
Processes 11 – 16

- Ash photoresist
- RCA clean
- Grow 240Å oxide (shown with thick black line)
- Anneal ion implantations under nitrogen atmosphere



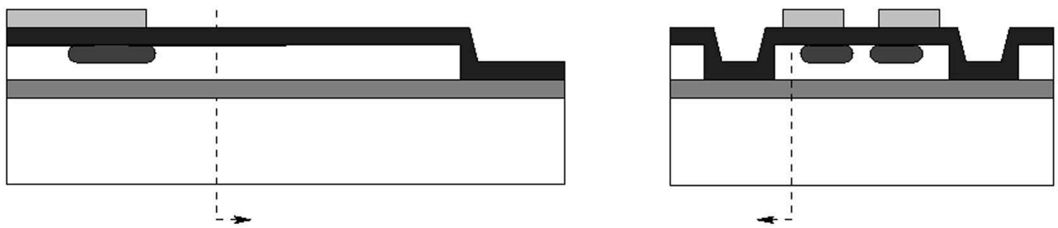
Processes 17 – 18

- Photolithography using Mask #3 (“Contact Holes Mask”)
- Open holes in oxide with BOE



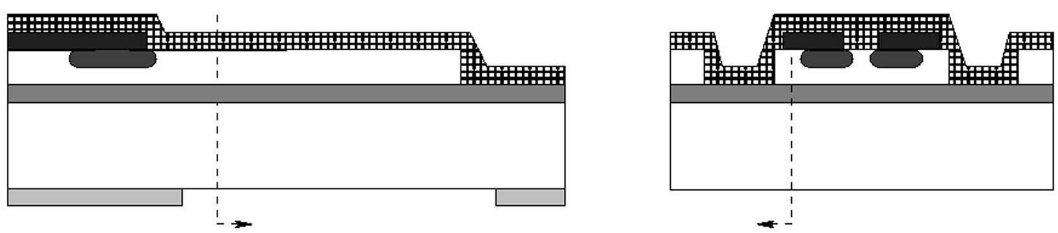
Processes 19 – 22

- Ash photoresist
- Pre-metal clean
- E-beam deposit 1 micron aluminum
- Photolithography using Mask #4 (“Metal Definition Mask”)



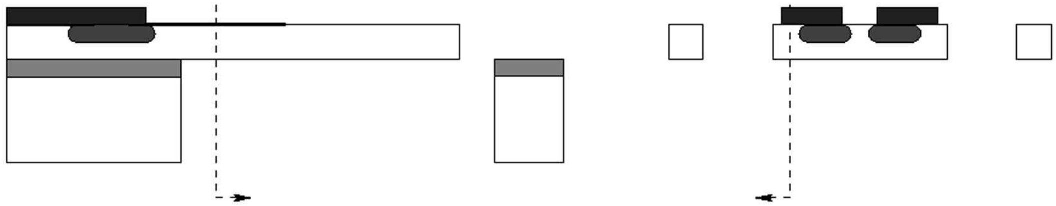
Processes 23 – 27

- PAN etch aluminum
- Ash photoresist
- Sinter aluminum contacts
- Frontside spin coat with polyimide and cure
- Backside photolithography using Mask #5 (“Deep Etch Mask”)



Processes 28 – 32

- DRIE etch through backside of wafer
- Ash backside photoresist and DRIE passivating polymer
- BOE embedded oxide layer
- Ash frontside polymide layer
- Die saw and wire bond to chip carrier



Fabrication Details

Ten SOI wafers were used in the final process flow. They were divided into three lots of 5, 3 and 2 wafers each. All ten wafers were subjected all process steps up to and including the piezoresistor definition step. However, only the first lot of 5 wafers was allowed to progress through the majority of the process flow. The remaining two lots were held back to be used in case something went wrong with the first lot.

First, the SOI wafers were RCA cleaned. Then a 240 Å ion-scattering oxide was grown on all the wafers. The wafers were then ion implanted with boron with an energy of 55 keV and a dosage of 5×10^{12} cm^{-2}. Simulation originally indicated that a boron dose of 5×10^{13} cm^{-2} annealed for 180 minutes at 1000 °C would give a good counter doping profile. Experimentally however, as explained in later sections of this paper, the results of the blanket doping were poor. In order to reduce the sheet resistance, we reduced the boron blanket doping. Once the wafers were returned, they were put through one piranha and one pre-metal clean to remove any surface contaminants.

There had been no problems in our experimentation with the resistor definition and arsenic implantation, so all the wafers went through this process at the same time. The wafers were coated, exposed to the "Piezoresistor Definition Mask", developed, and postbaked. The photoresist on one particular wafer, which was designated HAN30, did not adhere well to the silicon. This wafer had to be ashed and coated again because the coater was not working properly. Large areas of the resist lifted off, making the wafer unusable. It was discontinued as a product wafer. It was, however, implanted with arsenic, and will be sent out for concentration and resistivity profiling in the near future.

All of the wafers were then implanted with arsenic at a dosage of 10^{16} cm^{-2} at 20 keV by a commercial vendor. When the wafers came back, they were dipped in 7:1 BOE for 40 seconds to remove the oxide over the resistors. Even though the energy level for the arsenic implant was low, the current was high enough to heat and polymerize the resist. That made it difficult to remove the resist with ashing alone. The photoresist was most easily removed with a 15 minute piranha dip followed by 5 minutes in the asher.

At this point the lots were split and 5 of the original 10 wafers were held in inventory. Four wafers from the first lot were coated with two microns of photoresist and then exposed to the "Cantilever Definition Mask". The exposure and develop time for the first wafer was 75 and 120 seconds, respectively. However, these parameters were not sufficient for full development of the photoresist image. The remaining wafers were subjected to 80 seconds exposure and 140 seconds development. The wafers were then put through a 30 second BOE dip to remove the oxide over the area that was to be etched. The plasma etcher was originally slated to be used for cantilever definition. However, this machine proved unreliable for reasons that could not be determined. After sacrificing one device wafer to the Lam Model 480 Plasma Etcher, and having few spare wafers with which to determine the source of the problems, cantilever definition etching was completed on the remaining wafers using the STS DRIE etching machine. The wafers etched in the STS for 100 seconds using recipe MIT69. Two microns of silicon were etched away at a rate of about two microns per minute. Because the STS has a 70:1 selectivity of silicon over SiO_2 and photoresist, the wafers could be safely over-etched. After STS etching, the wafers were placed in the asher for two minutes to remove the photoresist. The wafers were then put through a RCA clean in preparation for putting them in the furnace. For 20 minutes of a 60 minute anneal, 240 Å of dry oxide was grown, at 1000°C. Except for the oxidation phase, the ambient for the anneal was N2. The wafers were then put back into the furnace to anneal for 120 min. at 1000°C in an N_2. The original anneal time for the arsenic was 120 minutes at 1000 °C. The measured junction depth for the 120 min. anneal was 0.2 microns on a bulk p-type wafer with a concentration of $8x10^{15}cm^{-3}$. To prevent spiking from the aluminum the minimum depth had to be at least 0.3 microns. For this reason, the arsenic anneal time was increased to a total time of 180 minutes at 1000°C. In the simulation, the junction depth was determined by the arsenic profile, not the boron, so the boron and arsenic anneal times were made identical.

The wafers were coated with one micron of photoresist and were exposed to the via mask. A one micron layer of photoresist left streaking on the wafers, and one or two dies on each wafer was not coated correctly. The streaking was caused by the two micron deep cantilever definition. The exposure and develop times were 55 and 90 seconds, respectively. It was learned from the DRIE group that photoresist remained in the trenches of the cantilevers if only a 45 second exposure and a 80 second develop time were used. Adding more time removed the unwanted photoresist and the mask features were not overdeveloped. Once they were developed and postbaked, the wafers were put into 7:1 BOE for 45 seconds to cut the contact holes. They were then put in the asher for 90 seconds. Next they went through a pre-metal clean. The wafers were then e-beamed, using program 1, with one micron of aluminum. While putting the wafers into the e-beam, one wafer fell on the floor and broke.

The three wafers were again coated with a one micron thick photoresist layer and exposed to the metal mask. Once the wafers were developed and postbaked they were put into a PAN etch. In previous experiments, the control etch time was 140 seconds, but in this run the etch time was 165 seconds. An additional 15 seconds was added to the time because the wafers were done in a batch and not individually. The wafers had residual aluminum on the edges of the trenches facing towards the wafer center, so the wafers were etched for an additional 20 seconds (see Figure 4). While the aluminum still remained, further etching was not done to avoid over-etching the wafers. The wafers were then ashed for 90 seconds and sintered for 47 minutes at 400°C: for 31 minutes under N_2 and H_2 and 16 minutes under no flow.

After these wafers were completed and passed on for polyimide spin on and backside etching, the other five wafers were started. Two of these wafers were to be done by the process described above, while the other three were to have the metal deposition and patterning done before the cantilever etch. Doing the cantilever etch after the metal would prevent aluminum deposition in the trenches. All five wafers proceeded through processing up to the e-beam, which failed after only a 0.1 micron layer of aluminum had been deposited. Failure was obvious, from smoke coming out of the e-beam. By this point the backside etch of one wafer had been successfully completed and production of the five remaining wafers stopped. These will be kept in inventory so that they can be completed later if necessary.

The three wafers received from piezoresistor implant and cantilever definition had their structures protected with a double layer of polyimide PI2545. A thick layer of photoresist would also have served to simply protect the structures. However, because PI has a residual tensile stress after curing, it helps to prevent extensive buckling when the oxide windows (under compressive stress) are opened during the DRIE process. Because photoresist also has residual compressive stress, it would not have afforded the same protections from buckling (see Figure 5 and Figure 6). The double PI layer was approximately 6.5 microns thick. Another version of polyimide, PI2721, which has higher viscosity, was tested on control wafers to determine if it would be useful as a single coat of thick protectant. We found that PI2721 inexplicably turned black, and left dark brown deposits on the wafer boat during the curing process. The manufacturer's technicians indicated that this should not have occurred. We tested their suggestion of increasing the N_2 flow in the cure tube, but with no success. Due to the time constraints of our process flow, and the proven use of a double layer of PI2545, we used the existing technique rather than risk device wafers.

To define the etch mask for the DRIE process, a layer of thick photoresist layer (AZ4620) was spun onto the wafer backside. Thickness was approximately 10 microns sufficient to survive the DRIE etch of 500 microns of silicon, with a selectivity of 70:1. The thick resist was patterned using the deep etch mask, IR aligning it with the metal layer. To completely expose the thick resist, an exposure of 500 seconds was required.

To prevent depositing PI on the STS chuck, a handle wafer was attached to the wafer front side using photoresist as a bonding agent (see Figure 7). A post bake of a few minutes is sufficient to harden the PR. On the first and third device wafers (322 ADU HAN 25, 124 ADU HAN 05), the bonding droplets may have been too small, preventing good thermal contact with the handle wafer and the STS chuck. As a result, we believe that the thick resist mask heated up, reducing the etch selectivity, and permitted complete removal of the resist, resulting in etching of the wafer backside. To provide good thermal contact between the device wafer and the handle, fairly large droplets of PR must be used, and the device wafer pressed firmly onto the handle. This was successfully performed on device wafer AD 1 HAN 23.

The deep etch of the device wafer was accomplished using the DRIE technique, for about 275 minutes, at an etch rate slightly less than 2 microns/min. As described, the selectivity of silicon over PR is highly sensitive to the temperature of the wafer. If temperature rises significantly, selectivity falls to a level where the PR will not protect the wafer and a scalloped wafer surface results. Only device wafer AD 1 HAN 23 survived the etch undamaged.

The each rate of the STS etcher was not uniform. In concave corners of the mask, some silicon remained in a thin layer. However, undercutting or footing occurred under convex corners and along long straight wall sections. For our devices, this meant that some silicon remained near the break-off legs, while the SOI oxide was undercut under the cantilevers (see Figure 8). The implication of this phenomenon is that DRIE should be performed until critical structures are properly etched, and then stopped. In our case, this would leave a thin membrane of silicon attached near the break-off legs, but this would be too thin to be consequential.

Once complete, the photoresist and any remaining passivant polymer layer were removed in a five minute oxygen plasma ashing. This step was essential in our process, as the timed DRIE etch may finish in either an etch cycle or a passivate cycle. Unless one observes the device state at the end of processing, it cannot be visually determined if the passivant polymer remains on the wafer (a fluorescence microscope may show this). If the passivant remains, it will not be attacked by the BOE, and will prevent the etching of the SOI oxide layer. Figure 5 is an image of a test wafer that was processed before this discovery, and had the polyimide removed before the oxide was successfully etched.

The wafer and attached handle were separated in a brief acetone dip. While the PR left residue on the wafer, at this stage it did not impede processing.

BOE was used to remove the oxide in the window surrounding the cantilevers. At approximately 800Å/min, etch time was 12 minutes. Good control of etch time should be maintained to prevent undercutting of the upper SOI silicon layer. This may be difficult to prevent if the DRIE process caused footing.

Another handle wafer was attached to the backside of the device wafer. This provided a gripping surface for the vacuum wand in the asher. Without the handle, the PI "windows" covering the cantilevers were sucked through the wafer when the vacuum was turned on, breaking off cantilevers in the process (see Figure 9). With the handle wafer, no damage to the cantilevers or PI layer windows occurred.

The front side was ashed to remove the PI as well as the previous handle wafer bonding PR. This typically takes longer than the backside PR ash, as the cured polyimide is more difficult to remove than hard-baked PR. Ten minutes in the asher was sufficient to remove all traces of PI and PR.

Optical inspection at this stage showed that the aluminum stringers around the cantilevers might have been turned into fine strands of black aluminum oxide (see Figure 8). They moved in response to slight air currents. An acetone bath for an extended period was used to remove the handle wafer and the remaining bonding PR on the wafer backside. It also removed most of the black strands.

With these steps complete, wafer AD 1 HAN 23 was ready for breaking the cantilever chips out, mounting them, and testing their mechanical and electrical properties (see Figure 10).

Figure 4 --- Cantilevers with aluminum stringers. The wafer center is towards the left in this image. Centrifugal force on the photoresist during spin-on drives extra resist into corners that face the wafer center, and are more resistant to development.

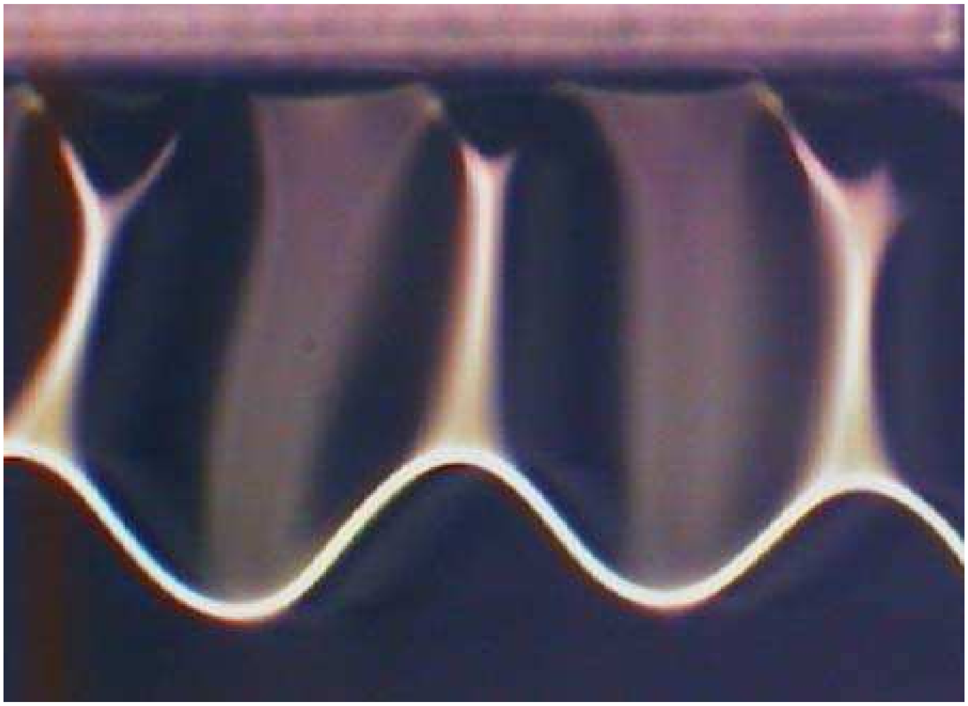


Figure 5 --- Highly buckled SOI oxide layer. A test wafer had PI removed prior to the oxide etch, so oxide is unrestrained from buckling. Note sharp peak of buckled membrane.

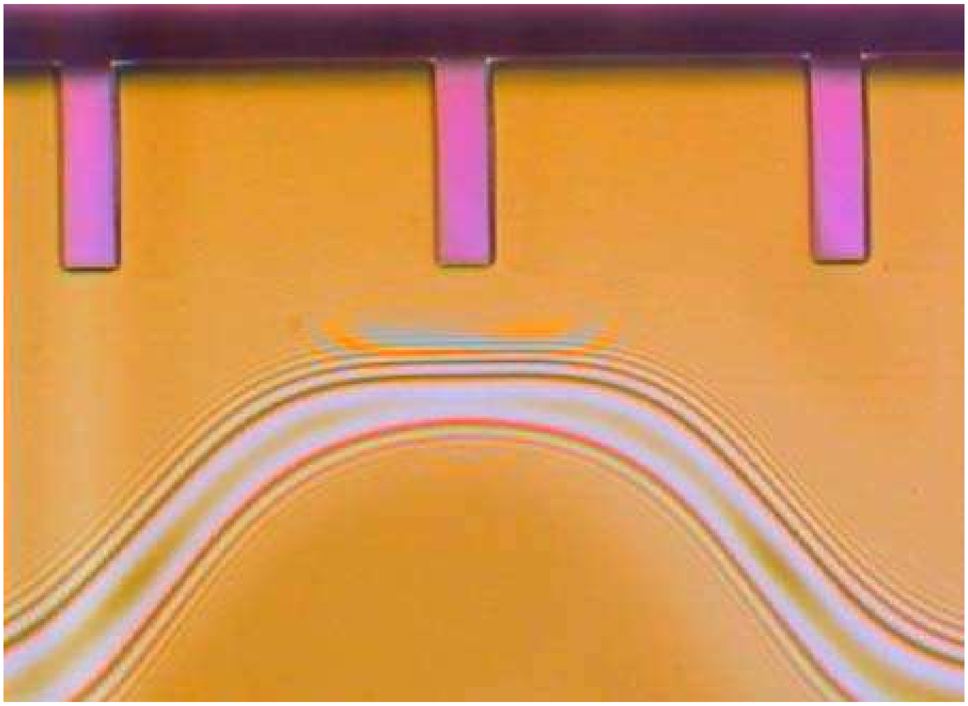


Figure 6 --- Slightly buckled oxide/polyimide membrane. With 6.5 μm PI over the oxide, the membrane buckles much less, and has smoother profile.

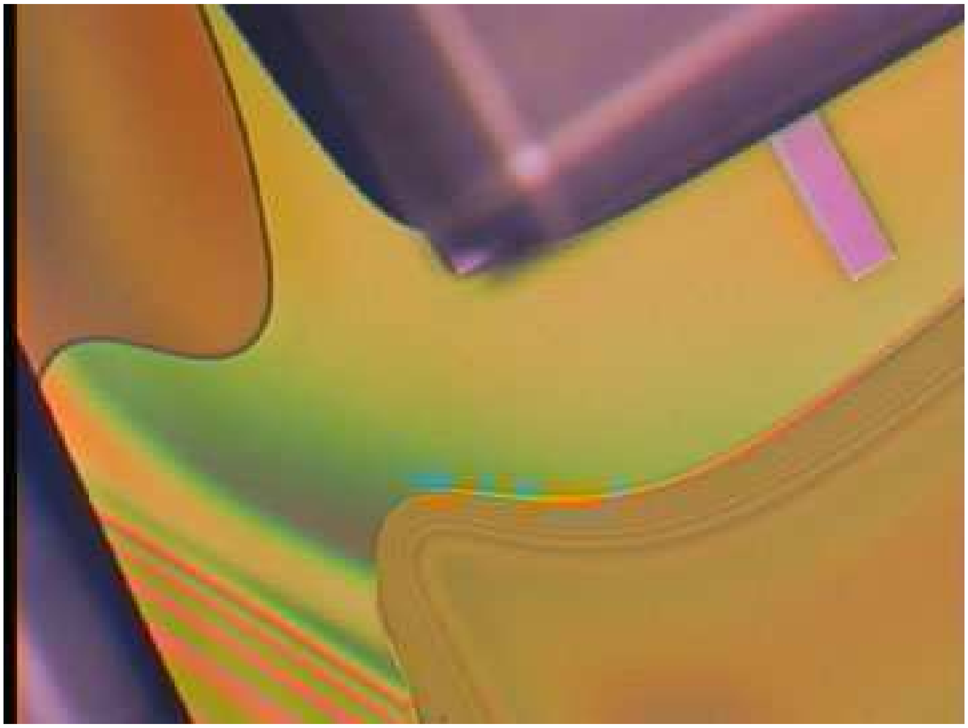


Figure 7 --- Photoresist bonding to front side of wafer. This view, through the backside window, shows where the photoresist bond pads are attached to the PI layer, and where there remains an air space

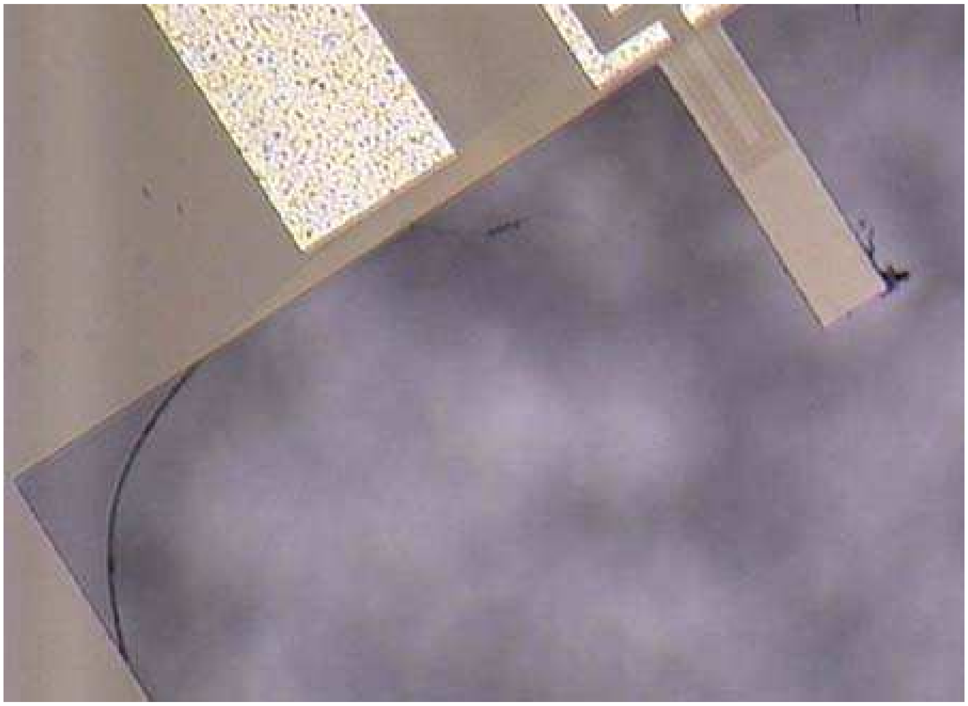


Figure 8 --- Footing and underetch from STS. The curved corner at the left is residual silicon, while the light region which extends the curve towards the cantilever, shows where only the top layer of silicon remains. Also note aluminum oxide residue attached to end of cantilever.

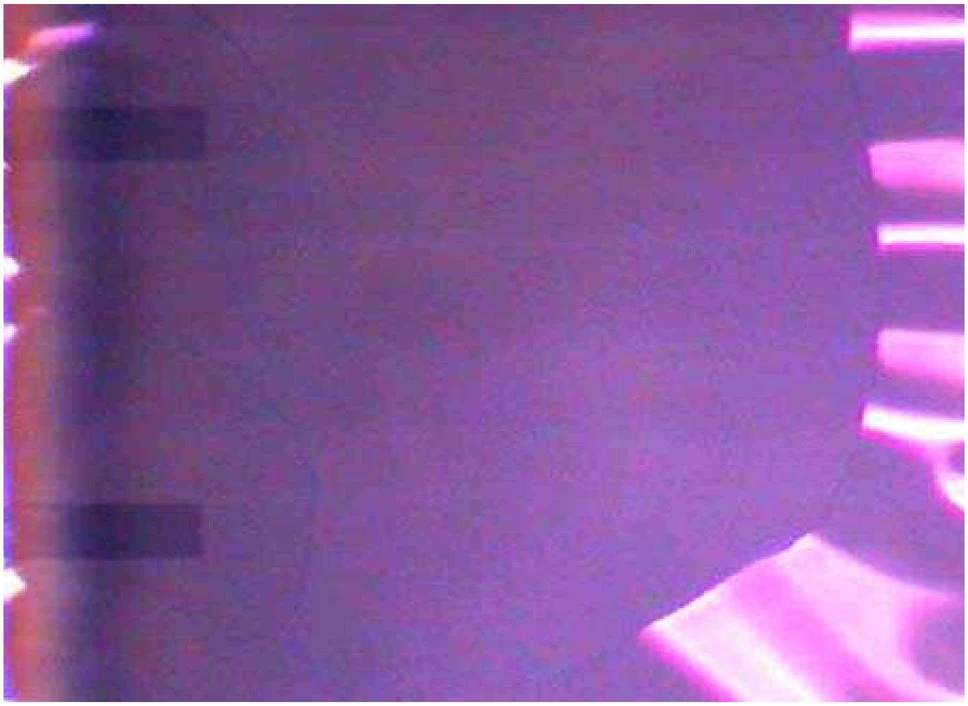


Figure 9 --- Suction damage. The membrane layer was shattered when the asher vacuum chuck picked up the wafer. In this example, the cantilevers at left actually reinforced the layer, and islands of the membrane remained around them.

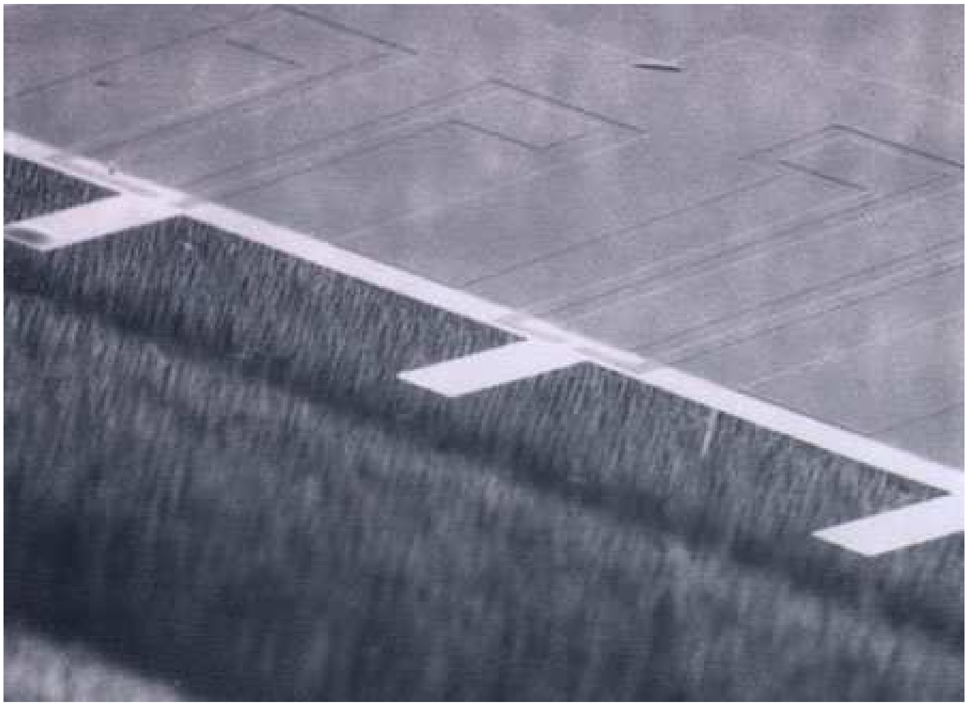


Figure 10 --- Completed piezoresistive microcantilevers. This SEM shows typical cantilevers, together with the aluminum contact pads. Note the undercutting of the cantilever silicon layer (white strip). This device was used in the resonant frequency tests. The leftmost cantilever has adhesive remaining on it.

Mechanical Theory and Characterization

Mechanical Theory

Derived from continuous beam theory, the natural frequency for the first mode of vibration for a simple cantilever beam can be written as:

$$f = \frac{3.52}{2\pi}\sqrt{\frac{EI}{\rho AL^4}} = \frac{3.52}{4\pi}\frac{t}{L^2}\sqrt{\frac{E}{3\rho}}$$

E is the young's modulus and ρ is the bulk density of silicon. For the first vibration mode, frequency is not a function of beam width. Since silicon is anisotropic, E should be taken in the direction of the beam. However, in this analysis, an average modulus over all crystal orientations is used.

Assuming the values shown below, an estimate of the natural frequency is *f* = 70 kHz:

$$E = 169GPa$$
$$\rho = 2330\,kg/m^3$$
$$t = 2\mu m$$
$$L = 200\mu m$$

Recasting the continuous form into a lumped parameter model, the system can be described by an equivalent mass and spring constant which are relevant over moderate displacements.

Equivalent mass of the cantilevers can be calculated by measuring the geometry of the beam. Errors in this analysis are linearly related to the errors in dimension measurements. In contrast, the linear component of the spring constant is proportional to the beam thickness cubed. As a result, experimental measurement is necessary to determine the actual value with good accuracy.

The equivalent mass for a cantilever beam can be expressed as

$$M_{eff} = \frac{3}{8}\rho wtL$$

where w is the width of the beam (50 microns). The effective mass M_{eff} is 17.5 nanograms. The stiffness of a cantilever beam is given by

$$k_{eff} = \frac{3EI}{L^3} = 2.11\ N/m$$

where

$$I = \frac{wt^3}{12}$$

However, this expression is highly sensitive to errors in the measurement of the cantilever thickness. Since the length scale is much larger, absolute errors in length measurement have a much smaller effect than do thickness errors. An alternative approach is to recognize that

$$\omega = \sqrt{k_{eff} / m_{eff}} \Rightarrow k_{eff} = (2\pi f)^2 m_{eff}$$

This gives an effective spring constant k_{eff} of 1.37 N/m.

Another technique makes use of the beam's resonant frequency, and the addition of a small additional mass. Consider:

$$\begin{aligned}
&\omega_1 = \sqrt{k_{eff} / m_{eff}} \qquad \omega_2 = \sqrt{k_{eff} / (m_{eff} + m_{add})} \\
&\Rightarrow m_{eff} = k_{eff} / \omega_1^2 \quad \Rightarrow k_{eff} = \omega_2^2 \left(\frac{k_{eff}}{\omega_1^2} + m_{add} \right) \\
&\Rightarrow k_{eff} = \frac{m_{add} \omega_2^2}{1 - \omega_2^2 / \omega_1^2}
\end{aligned}$$

This derivation provides the value of k_{eff} based on measurements of the resonant frequency and the value of an additional mass. The resonant frequencies can be accurately measured, but the mass value may be subject to estimation errors.

These derivations make certain assumptions. First, the calculations are based on the assumption of linearity. For large amplitude oscillations, the spring constant will change. For this reason, the measured resonant frequency could be slightly higher than that which would result from small amplitude displacements. Secondly, since the tests are performed in air, there will be damping effects. This can be observed in the frequency response plots, which show that the resonant peak magnitude is only a few times larger than the off-resonance response. Damping will tend to reduce the measured resonance from the undamped value. The relative contributions due to linearity and damping are difficult to determine, primarily because the fluid mechanics calculations around the beam are complicated due to the time varying "wall" locations.

One calculation which can be performed to provide first order confirmation of the measured values is comparison of the mass calculated based on measured geometry, and mass calculated by substituting the spring constant back into the expression for resonant frequency. If these are close to each other, it suggests that both the measurement and the calculated values are valid.

An interesting additional experiment would be to deflect the beam with a probe, draw the probe over the end of the cantilever and observe the resonant decay. This would provide information of the damping characteristics of the beam in air, as well as confirmation of the damped resonant frequency. However, this test was not performed during the course of this work.

Mechanical Characterization

The resonance technique described earlier was used to evaluate the (damped) natural frequency of the cantilevers. The facilities available to us to perform the resonance measurements were a Digital Instruments Nanoscope D3000 atomic force microscope in the Digital DNA Laboratory of the MIT Media Lab. This AFM measured the deflection of a cantilever by observing the location of laser light reflected from the cantilever. To excite resonance, the chip was mounted on a piezoelectric stack driven with a voltage "chirp". By comparing observed deflection vs. frequency, the resonant peak was easily determined.

A typical plot of amplitude and phase vs. frequency is shown in Figure 11. The resonant frequency in this plot is 44.4883 kHz. This is significantly lower than that expected from the theoretical value of 70 kHz. Possible explanations include the undercutting of the SOI silicon layer, which would increase the effective length of the cantilever, and imprecise values for the thickness of the cantilever. Based on these results and the previously estimated effective mass, the spring constant, k_{eff}, of the beam would be 1.37 N/m.

The additional mass for the second resonance test was provided by attaching a glass bead between 10 and 30 microns in diameter to the end of the cantilever with an adhesive. By performing a post-test SEM of the cantilever with attached bead, the size and mass of the bead was to be determined. Unfortunately, during transit, the bead became detached, leaving only the adhesive, so no calculations could be made. If it had, the bead volume could have been determined, as well as the amount of adhesive (by estimation). The resonant frequency was found to be 39.6641kHz. If the stiffness calculated above was correct, the additional mass of the bead and adhesive would have been:

$$m_{add} = k_{eff} \frac{\left(1 - \omega_2^2 / \omega_1^2\right)}{\omega_2^2}$$
$$= 4.53\text{ng}$$

We also measured the out-of-plane deflection of the beam for the no-load case. At the tip, the cantilevers typically rose 7-10μm above the plane of the wafer. This could be due to the presence of an intermediate Si-SiO_2 layer on the bottom surface of the cantilever.

If it was not entirely removed during the final HF dip, then a thin region with residual compressive stress would tend to deflect the beams upwards. Calibration of the device would make any effects of the residual beam curvature unimportant in measurement applications.

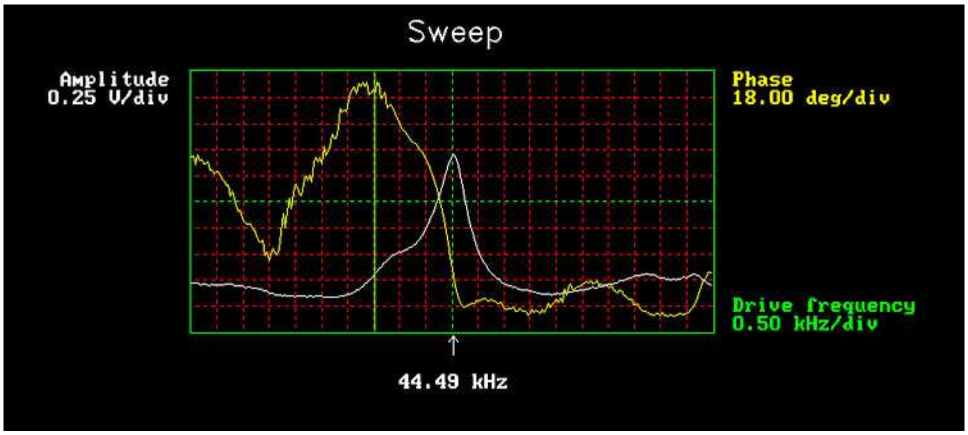


Figure 11 --- Gain phase plot for a piezoresistive cantilever when subjected to a frequency sweep. The damped natural frequency is 44.49 kHz.

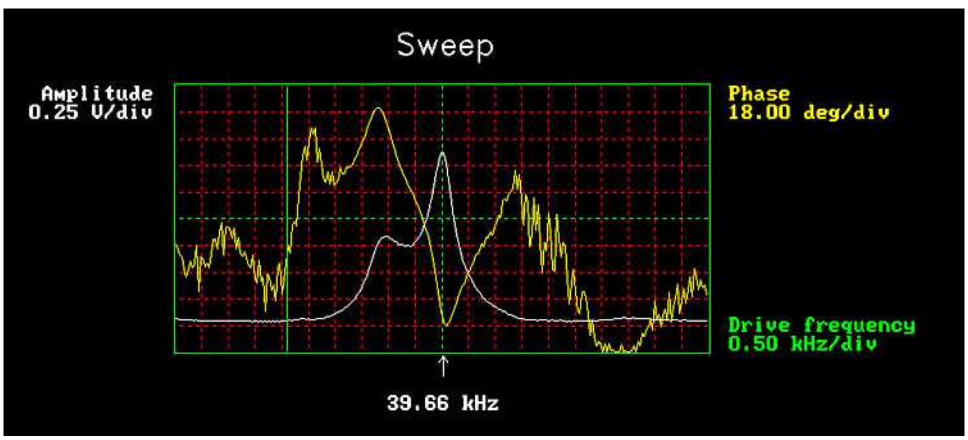


Figure 12 --- Gain phase plot for a piezoresistive cantilever with an attached glass bead (10 - 30 microns dia.) when subjected to a frequency sweep. The damped natural frequency is 39.66 kHz.

Electrical Theory and Characterization

Electrical Theory

A piezoresistor embedded in a thin cantilever beam must be localized as close to one surface of the cantilever as possible for maximum sensitivity. A choice must also be made as to the dopant type and resistor orientation to achieve good sensitivity. In the <110> direction, along the length of the cantilevers, the piezoresistive coefficient of N-type silicon is greater than that for P-type. Because arsenic atoms are larger, they are more easily contained to a shallow junction depths than boron, at reasonable implantation energy levels. For these reasons, the decision was made to blanket dope the wafers with boron and then to define the piezoresistors with arsenic. Achieving the necessary resistance, while minimizing the resistor length defined the dimensions of the resistor. The resistors defined in the Nishimoto mask set extend from the bulk silicon 90 microns, turn around and return. The original goal was to have piezoresistors of roughly 2.5kΩ. The resistor geometry yields approximately 40 squares with two legs 90x5 microns and a turn around of 20x5 microns. The target sheet resistance was therefore 62.5Ω/square. One concern with this configuration was that there might be leakage current from one leg of the resistor to the other. This would have a dramatic effect on the behavior of the piezoresistor.

The sensitivity of a piezoresistor varies proportionately to the thickness *t* and the radius of curvature. The Gage Factor, *GF*, is proportional to Young's Modulus, *E*, which is intrinsic to the material. Silicon is an anisotropic material but an average over all crystal orientations is E = 169GPa. The gage factor can also be calculated directly by straining the cantilevers and measuring the resistance change.

$$GF \cdot \varepsilon = \frac{\Delta R}{R}$$

Where ε is the strain in the material and R is the resistance. For a sensitive device, the gage factor should be on the order of 100.

Our process provided two methods for straining the piezoresistors. One was to bend a test wafer before the microcantilever has been released from the substrate. This could be done by bending a strip of silicon wafer against a test jig with a known curvature. Since the wafer thicknesses were known, the strain could be calculated.

Another method for measuring the gage factor was to use an atomic force microscope to bend a released cantilever by a known amount. From the deflection, the strain can be determined, and from resistance measurements the gage factor can be calculated.

Electrical Characterization

The electrical characterization describes tests done on the piezoresistors and other test devices on the wafers. Only the measurements for the SOI wafers that completed the piezoresistor definition through to the aluminum etch process are reported here. These wafers are designated as follows:

- Wafer HAN 07. This wafer has a junction depth of 0.2 microns and was implanted with boron with a dose of 5×10^{13} cm^{-2}. The arsenic implant dose was 10^{16} cm^{-2}.

- Wafer HAN 32 has a junction depth of 0.6 microns and was implanted with a boron dose of 5×10^{13} cm^{-2}. Wafer HAN 32 broke into two pieces while going through the PAN etch step. One piece was cut up with a die saw, and the other stored untouched. These two pieces had the same arsenic implant dose but a longer anneal time than HAN 07.

The measured results are interesting but not what was expected. The measured sheet resistance for HAN 07 was 250Ω/sq. Since this was above the desired sheet resistance the blanket boron doping for the production run was lowered by an order of magnitude. Interestingly, the sheet resistance of the HAN 32 wafer was 14Ω/sq (see Table 1). Nevertheless, when we measured the piezoresistors they had a *higher* resistance (see Table 2). The non-uniformity in the resistors indicated that there was another mechanism working here. The current might not always follow the path of the n-type resistor. Some current might also be flowing through the boron-doped space between the resistors and to ground.

The piezoresistors are unlikely to have large voltage potentials put across them in actual operation. However, punch-through voltage potentials were measured are presented in Table 3.

In order to get an estimate of the gage factor without having to test the cantilevers, a test jig was built which induced a known stress on the device. Figure 13 shows the test jig and a strip of silicon under applied stress. The clamps are round to insure that the point contact can be assumed. The test jigs were designed to provide known surface strains to 500 microns thick wafers. Other wafer thicknesses could be used, but strain would need to be recalculated. It is important to note that this strain technique produced a different strain than would actually be measured by a free microcantilever. When a whole wafer strip is put into bending, the stress profile extends through the whole wafer, so the surface strain can be considered to be nearly uniform. When a cantilever is bent, the stress varies significantly over the thickness of the piezoresistor. In fact, if the piezoresistor extends below the neutral axis of the beam, this lower region will change resistance in the opposite sense from the upper region. Therefore, it was expected that the strain measurements done with the test jig should give higher gage factor values than the actual cantilever would give.

It was very disappointing to find that there was no measurable resistance change using HAN32 when put under 1000 microstrain (see Table 4). This is a level which is approximately 10% the theoretical fracture point of silicon. The wafer broke when placed on a test jig that caused 2000 μ strain. Microfeatures on the surface of the jig might have initiated a fracture in the silicon.

The equation used to calculate oxide thickness is $t = A\varepsilon/C$, where t is oxide thickness, A is area of the capacitor in the diode structure, ε is the permittivity, and C is the capacitance. The calculated oxide thickness values of 430 and 539 Å correlate well with the measured oxide thickness value of 480 Å from the control wafers (see Table 5).

In testing the diodes (see Table 6), it was found that they behave more like resistors. This is most likely due to the blanket doping. The boron doping might not have been uniform, allowing the concentration to be very low compared to the arsenic concentration. Having such a low concentration increases the depletion width dramatically, allowing current to flow easily through the diode.

In preparing the wafers for testing, the die saw left residue on the wafer, but it did not effect the contact resistance measurements; the probes could be used to scrape the dirt off and make good contact to the aluminum surface (aluminum contact resistance shown in Table 7).

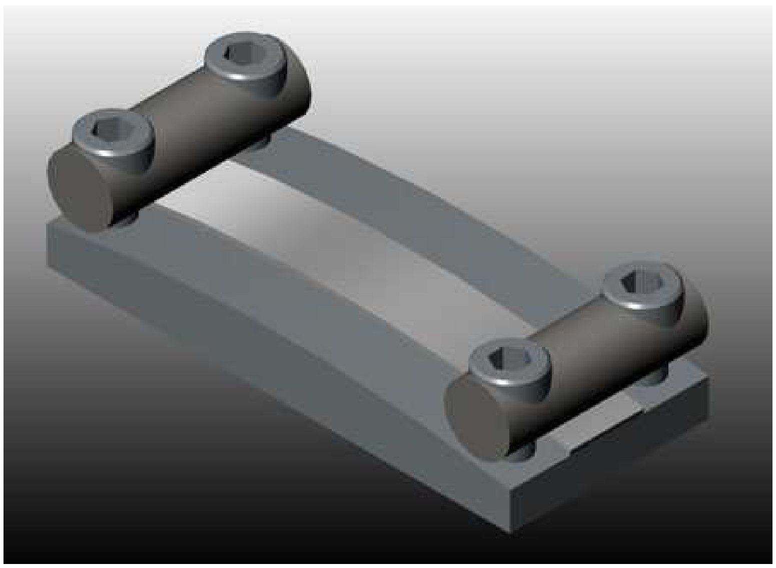


Figure 13 --- Jig for testing the piezorestivity of the resistors while under applied stress

Table 1 --- 32 square resistor

	SOI HAN 32 Big piece	*SOI HAN 32 Diesaw piece*	*SOI HAN 07*
32 square resistor	14.7 kΩ	10.5 kΩ	912 Ω
Resistance (Ω / □)	459	328	28.5

Table 2 --- Cantilever Resistors

Resistance (kΩ)	*SOI wafer HAN 32 Big piece*	*SOI wafer HAN 32 diesaw piece*	*SOI wafer HAN 07*
Resistor 1	20.6	14.2	1.18
Resistor 2	12.7	19.8	1.27
Resistor 3	23.8	15.2	0.9
Resistor 4	23.8	17.8	1.2
Resistor 5	13.8	15.8	1.14

Table 3 --- Punch through voltage of cantilever resistors using the same resistors as above

	SOI wafer HAN 32 Big piece	*SOI wafer HAN 32 diesaw piece*	*SOI wafer HAN 07*
Resistor 1	16.5 V	16 V	9.5 V
Resistor 2	17 V	16 V	9.5 V
Resistor 3	16 V	16 V	9.5 V
Resistor 4	16 V	16 V	9.5 V
Resistor 5	17 V	16 V	9.5 V

Table 4 --- Gauge Factor measurements of HAN 32 diesaw piece

Resistance (kΩ)	*0 strain*	*1000 μ strain*
Resistor 1	18.3	18.3
Resistor 2	8.8	8.8
Resistor 3	25.8	25.7

Table 5 --- 500 x 500 μm parallel plate capacitor

	SOI HAN 32 Big piece	*SOI HAN 32 Die saw piece*	*SOI wafer HAN 07*
Capacitance at 1 MHz (pF)	5.2	4.8	15
Capacitance at 200 kHz (pF)	22	24	32
Capacitance at 20 kHz (pF)	165.6	149	258
Capacitance at 10 kHz (pF)	200	160	258
Calculated oxide thickness (Å) at 10 kHz	430	539	334

Table 6 --- Diodes in forward bias

	SOI HAN 32 Big piece	***SOI HAN 32 Die saw piece***	***SOI wafer HAN 07***
Threshold Voltage	112 mV	102 mV	152 mV
Current at 1 volt	632 µA	598 µA	3800 µA
Current at .5 volts	257 µA	248 µA	1500 µA
Current at -1 volt	159 µA	220 µA	2100 µA
Current at -.5 volts	79 µA	116 µA	800 µA

Table 7 --- Aluminum contact resistance

	SOI HAN 32 Big piece	***SOI HAN 32 Die saw piece***	***SOI wafer HAN 07***
Resistance (Ω)	5.0	2.5	2.4

Device Performance Characterization

The completed and mounted cantilevers, were inserted as one leg in a Wheatstone bridge circuit, as shown in Figure 14. Using the AFM described earlier, the cantilevers were deflected through a small range of displacements while the bridge voltage was measured.

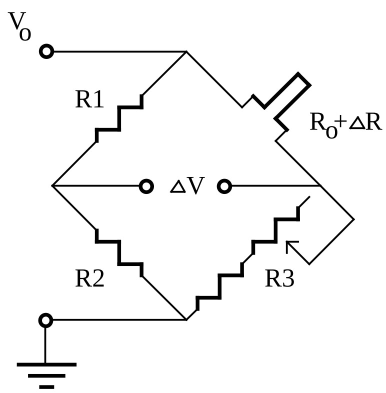


Figure 14 --- Wheatstone bridge circuit: R_1=9.93k, R_2=9.97k, R_3=10.1k, R_0=10.6k

$$\Delta V = V_0\left\{\frac{R_2}{R_1+R_2} - \frac{R_3}{R_0+\Delta R+R_3}\right\} \Rightarrow R_0+\Delta R = R_3\left\{\frac{V_0\left(R_1+R_2\right)}{R_2V_0-\Delta V\left(R_1+R_2\right)}-1\right\}$$

Using this equation, the net resistance can be determined. *ΔR* found in relation to the undeflected resistance R_0 can also be determined. Fractional resistance change $\Delta R/R_0$ vs. tip deflection is shown in Figure 15, and has a slope of 0.51% change in resistance per micron of tip deflection. The bridge unbalance voltage has been removed in these calculations.

From these values and the earlier expression for Gage Factor, and assuming constant curvature in the beam we obtain:

$$GF = \frac{\Delta R/R}{\varepsilon} = \frac{\Delta R/R}{t/2r}$$

For an end-loaded cantilever beam, with deflection δ_{max} at the end, and length *l*, the equation describing its shape and curvature are (*x=0* at cantilever tip):

$$\delta(x) = \delta_{\max}\left(1-\frac{3}{2}\frac{x}{L}+\frac{x^3}{2L^3}\right)$$
$$\Rightarrow \left|\frac{d^2\delta(x)}{dx^2}\right| = \left|\delta_{\max}\left(\frac{3x}{L^3}\right)\right| \approx \frac{1}{r}$$

So the gage factor for a resistor placed at the root of the cantilever is:

$$GF = \frac{\Delta R/R}{t/2}\frac{L^2}{3\delta_{\max}} = \frac{\Delta R/R}{\delta_{\max}}\frac{2L^2}{3t} = 0.0051\mu m^{-1}\frac{2(200\mu m)^2}{3\cdot 2\mu m} = 68$$

Since the piezoresistors are not located at the root of the cantilever, the local curvature will be lower, meaning lower strain, and a higher actual gage factor. This indicates that our earlier estimate of *GF=100* was of the right order of magnitude.

Due to the difficulties encountered during the measurement of the test wafers, valid comparisons cannot be made with those gage factor calculations.

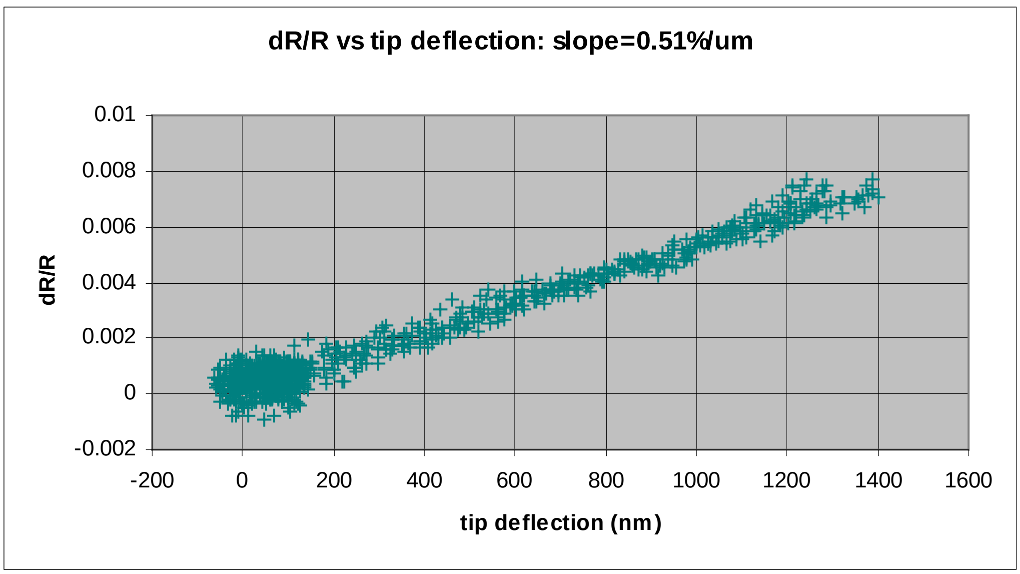


Figure 15 --- Fractional resistance change vs. microcantilever tip deflection.

Suggested improvements and further discussion

The main source of the resistor non-uniformity problem is likely to be the blanket counter-doping. The test device diodes behaved more like resistors, allowing an unacceptable reverse bias current to pass through. The resistors were also found to be leaky. The best solution to these problems is start with SOI wafers that have the desired doping type and concentration to avoid the blanket counter-doping that was necessary for these wafers.

Improved p-n junction quality would reduce the variance of the resistors and probably improve the gauge factor as well. With improved junctions the current would follow the path of the resistor rather than leaking across the path between the legs of the resistors.

Properly pre-doped wafers were not available at the beginning of the project. If we had realized how difficult the doping and counter-doping would be, we would have focused more of our efforts on insuring that functional devices were being built on the test wafers. Not enough time was spent in the early phases on testing wafers.

In order to test the wafers on the strain gage die, they were cut up into strips using a die saw. While this method was convenient, it also caused problems, such as the deposition of residue. If strips are required in future work, they should be cleaved instead. When the die saw was used on the experimental wafers it left a residue that could not be taken off with even with nanostrip. Most likely the residue was silicon dust left from the die saw. Cleaving the wafers would eliminate the residue, leaving the aluminum contacts clean. Another solution would be to cover the wafer with photoresist or some other material before sawing. The problem with this method it that in the final product the holes all the way through the wafer would make it difficult to fully coat the wafer.

Fortunately, in the mask design, half of the dies do not need to cleaved or die-sawed. They were designed to be broken out with tweezers. As a recommendation for a future mask set, each of the dies should be designed with this feature in mind.

Another change in the process flow that we recommend is that the aluminum should be e-beam deposited and etched before the cantilever etch is defined. The cantilever definition etch leaves a 2 micron trench. The photoresist that forms the aluminum etch mask collects more deeply along inward-facing edges during spin-on. Because of this the exposure is shorter than necessary for the rest of the resist, and some remaining resist protects the aluminum in these regions. By depositing the aluminum before the cantilever definition etch, there will be no trenches to collect aluminum or photoresist.

For the existing process, the develop and etch times need to be balanced in order to remove the trench resist while not over-etching the flat sections. We did not do this well and there was residual aluminum left on the sides of the trenches of the device wafers. There was, however, only a small amount of aluminum left so when the cantilevers were released from off the oxide, most of the aluminum came off. It would be better for it not be there in the first place.

The alignment marks on the masks could be improved. Having only two alignment marks on each die led to some masks being exposed half a die from the correct location. In addition the alignment marks become confusing after several lithography steps. The easiest way to align the mask and the wafer was to roughly align the cantilevers and then look at which boxes were almost aligned. The alignment marks on the dark field via and active masks should have a clear window around them to improve visibility. This would allow for easier alignment.

In terms of the structure of the cantilever, one suggestion would be to have a split leg cantilever with the piezoresistor running up one leg and down the other. This would do two things: first, there could be no leakage current in the across the legs of the piezoresistor because of the physical barrier; second, the split leg cantilever would have a lower spring constant. While this would lower the natural frequency it would increase the sensitivity of the device. Split leg cantilevers are not new and are the primary construction geometry for AFM tips.

In the early stages of testing the DRIE using polyimide on the front side of the wafer, other STS users complained that our wafers were leaving residue on the chuck. To solve this problem, we attached the polyimide side of the wafer to a handle wafer using photoresist as an adhesive. When doing this the first time, very little photoresist was used. While the handle wafer stayed attached to the device wafer, the thermal conductivity was very poor. During the DRIE ion bombardment, the device wafer could not dump enough heat through the handle wafer. This heating made the photoresist on the front side of the wafer less resistant to the etcher, and the wafer surface was damaged. When larger drops of photoresist on the second device wafer, the etching was completed without damage. For future reference, good contact should be made between the device and the handle wafer.

The STS etcher has two modes of operation. One is an ion bombardment and the other is the deposition of a passivant polymer. These two modes cycle at roughly 30 second intervals. When the etch time elapses the machine stops in whatever cycle is active. If the machine was in the polymer deposition phase, then there will be polymer left on the device. As a preventative measure, ashing the wafer before the BOE step removes any passivant that would have blocked etching of the oxide. This is done with a handle wafer still attached to the wafer to prevent suction damage to the polyimide layer and the cantilevers.

After releasing the cantilevers, SEM images show that the cantilever roots were undercut by several tens of microns during the DRIE process. The inside, concave corners, however, were under-etched. Because precise realization of the inside corners of the deep etch windows is not critical to device performance, the DRIE etching process should be stopped when the root of the cantilever is flush with the side walls of the window.

Appendix A: Detailed Process Flow

- RCA clean
- Grow 240A of oxide. 20 minutes dry O_2 at 1000 °C using recipe 121
- Ion Implant with Boron. Implant dosage is 5×10^{12} cm^{-2} at 55 keV
- 2 Piranha cleans (10 minutes each) and one 15 second HF dip at the end
- HMDS at 150 °C
- Coat with 1 um Olin positive photoresist 820 35 cs
- Expose with Mask #1 ("Piezoresistor Definition Mask") for 45 seconds in soft contact
- Develop in 3:2 OCG934 developer for 80 seconds and postbake for 30 minutes
- Ion Implant with Arsenic. Implant dosage is 1×10^{16} at 20 keV
- BOE 7:1 for 40 seconds to remove oxide over resistors
- Piranha for 15 minutes
- Ash wafers for 5 minutes
- HMDS at 150 °C
- Coat with 2 um of photoresist using line 16 of the ICL coater
- Expose to active mask (cantilever definition) for 80 seconds in soft contact
- Develop in 3:2 OCG934 developer for 140 seconds
- Postbake for 30 minutes
- BOE in 7:1 for 30 seconds
- DRIE for 1:40 minutes. 2 um etch recipe MIT69. SF_6 etch gas and C_4F_8 passivating gas. Etch rate about 2 um per minute.
- Ash for 2 minutes
- RCA
- Grow 240A of oxide. 20 minutes dry O_2 at 1000 °C using recipe 121 (includes 60 minutes of anneal time)
- Anneal arsenic and boron implantations for 120 minutes in N_2 at 1000 °C. Used recipe 259. (Total anneal time is 180 minutes at 1000 °C)
- HMDS at 150 °C
- Coat with 1 μm Olin positive photoresist 820 35 cs
- Expose to via mask (contact holes) for 55 seconds in soft contact
- Develop in 3:2 OCG934 developer for 90 seconds
- Postbake for 30 minutes
- BOE in 7:1 for 45 seconds
- Ash photoresist for 90 seconds
- Piranha clean for 10 minutes and 15 seconds HF dip
- E-beam wafers with 1 μm Al. Used program 1, film 1. Changed predeposit time to 40 seconds instead of 20 seconds
- Coat with 1 μm of Olin positive photoresist 820 35 cs
- Expose to metal mask for 55 seconds in soft contact
- Develop in 3:2 OCG934 developer for 90 seconds
- Postbake for 30 minutes

- Pan etch Al at 40 °C. Etch batch (4 wafers) for 3 minutes. Added an additional 15 seconds from the control time because the wafers were in a batch
- Ash for 90 seconds in asher
- Sinter for 47 minutes at 400 °C. 31 minutes under N2/H2 and 16 minutes under no flow.
- VM652 adhesion promoter spin on, 5sec @ 1000rpm, 30sec @ 4000rpm
- Solvent drive off, 120 °C hotplate for 60 sec
- PI2545 1st coat spin on, 15sec @ 1000rpm, 30sec @ 1500rpm
- Softbake, 130 °C oven, in boat, 30 minutes
- Cure, N_2 ambient, 350 °C for 45 minutes
- PI2545 2nd coat spin on, 15sec @ 1000rpm, 30sec @ 1500rpm
- Softbake, 130 °C oven, in boat, 30 minutes
- Cure, N_2 ambient, 350 °C for 45 minutes. At this point the double coating of polyimide was measured to have an average thickness of 6.5 microns.
- HMDS cycle at 150 °C
- Thick resist (AZ4620) application: 9sec @ 1750rpm spread, 60sec @ 1000rpm spin, 6sec @ 5000rpm
- Prebake, 30 minutes
- IR align and expose back side using default mask (deep etch mask) 500sec
- Develop in AZ440MIF for 4 minutes 15 seconds
- Spread thin layer of resist along edge of wafer to reinforce thick resist in the DRIE etcher
- Attach front side to handle wafer using photoresist bond pads. Creating large bond photoresist bond pads is absolutely critical to prevent thermal breakdown of the thick backside resist during the DRIE etching procedure.
- Postbake, 5 minutes.
- DRIE in STS machine for 275 minutes, 500μm, recipe MIT69, but with platten RF power reduced to 80W
- Ash twice in ICL asher: once for 5 minutes, again for 1 minute
- Acetone bath to separate handle wafer from device wafer
- BOE in 7:1, 12 minutes with gentle agitation
- Postbake, 5 minutes to evaporate water in etch cavities
- Attach handle wafer to backside of wafer. Size of photoresist pads is not critical, as only ashing will be performed.
- Ash in ICL asher, 10 minutes
- Acetone bath to separate handle wafer and dissolve remaining PR
- Postbake, 5 minutes to evaporate water in etch holes
- Break 3-cantilever die segment out of the wafer
- Wire bond cantilever chip into chip carrier