The Design of a High Performance Simultaneous Bidirectional MOS Driver

by

Kin Hong Kan

Submitted to the Department of Electrical Engineering and Computer Science
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"Of making many books there is no end,
and much study wearies the body."

Ecclesiastes 12:12b, NIV.

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Chapter 1

Introduction

This thesis describes the design of a high performance simultaneous bidirectional MOS driver. The driver allows point to point digital signal transmission across chips in both directions, over the same pin, at the same time. The driver's noise isolation features allow the signalling method to operate at high speed.

This chapter describes the motivation for a simultaneous bidirectional driver, and previous research being done on the topic. Chapter 2 provides the system overview of the driver. Chapter 3 details the design of the receiver circuit. Chapter 4 discusses the effects of the chip package on the driver, and the design of the transmitter circuit. Chapter 5 describes the performance of the driver as shown by simulation results. Chapter 6 describes the implementation of a driver test chip on a 1.2μm process. Finally, Chapter 7 provides a conclusion of the design and suggestions for future improvements.

1.1 Motivation

As fabrication technology advances, we are capable of putting more and more transistors onto a single chip. The limiting factor for the amount of logic in a single package thus gradually shifts from the die area to the number of I/O terminals available. The naive interpretation of the Rent's rule below give us a feel for the terminal requirement as technology advances.

$$N = aB^b \tag{1.1}$$

where N is the number of terminals for a package, B is the number of logic blocks in the package, a is the average number of terminations per block, and b takes a value between 0.4 and 0.7. [8]

VLSI sizing rule tells us that circuit density increases with the square of the feature size reduction ratio. This is the same as saying that B increases 4 times as the the feature size decreases by one half. Depending on b's value, the corresponding increase in terminal requirement thus amounts to 1.7 to 2.6 times. The simple calculations implies that designers would need about twice as many terminals for a package, if they want to give up the aging 2μm process and take full advantage of a 1μm process.

Smaller pins and other advanced packaging technology, such as the IBM C4 chip attachment process, [1] have been employed to provide the required chip terminals. This thesis, however, describes a simultaneous bidirectional driver which doubles the chip-to-chip bandwidth without increasing the number of chip terminals. The driver allows simultaneous bidirectional digital signalling over the same pin. It enables us to stay with relatively simpler and cheaper packaging technology as we pack more logic onto one chip.

An application of the simultaneous bidirectional drivers is the interconnection of routers in a multi-processor computer. In a simple 3D mesh network, each router is connected to 6 other routers, and each of the interconnection requires a pair of bidirectional data paths. Therefore, excluding control signals, a 16-bit data path would amount to 192 terminals, and a 32-bit data path would result in 384 terminals. Simultaneous bidirectional drivers are capable of reducing the above numbers by one half, which allows the use of cheaper and simpler packages. The reduction in the number of pads also implies a reduction in chip area, since many routers are pad-limited.

[1] The IBM C4 chip attachment process allows chip pads to be located throughout the die, instead of just the periphery. The process releases the constraint on the number of chip terminals imposed by the perimeter size of the die.

1.2 Previous Research

Experimental simultaneous bidirectional drivers have been built and shown to work at 100 MBits/s on a 2μm CMOS process. [9, 10, 6] These drivers are characterized by their current mode operation and small voltage swing. Techniques for noise reduction, such as on-chip termination control and rise-time control have been explored. The design of the simultaneous bidirectional driver in this thesis also employs the above techniques, together with the mechanism of current steering. By using a 0.8μm CMOS process, simulation results indicate that the driver will operate at 400 MBits/s.

Chapter 2

System Overview

The simultaneous bidirectional signalling method described in this thesis is derived from the work of a previous design[6]. The methodology that allows the signalling method to operate at high speed, even with relatively noisy ground and power supplies, is current mode signalling. This chapter gives an overview of current mode signalling and the application of the method to bidirectional signalling.

2.1 Current Mode Signalling

2.1.1 Noise in High Speed Digital System

As digital design engineers are riding the technology curve, they are given transistors that have higher and higher gain-bandwidth product. Their digital systems are no longer bound by the performance of the devices; rather, by the performance of the interconnections[5].

Real world interconnections, including chip package leads, wires and circuit board traces, behave as distributed inductors, capacitors and resistors. Traditional digital systems make use of voltage level signalling. A logic 1 or logic 0 is defined as a relative voltage to a ground plane that is being distributed to the whole digital system. This causes a problem when a large amount of inter-chip drivers are driving signals with high voltage swing at high speed. The change in power supply current to these drivers

Figure 2-1: A Current Mode Signalling System

causes noise in the power and ground planes, governed by $\Delta V = Ldi/dt$. Noise in these voltage reference planes thus limit the speed of a voltage level signalling system.

2.1.2 Current Mode Signalling

Figure 2-1 shows a current mode signalling system that solves the power supply noise problem. In the model, a chip package lead is modeled as an inductor while a circuit board interconnection is modeled as a transmission line.

In a current mode signalling system, a logic 1 is transmitted as as a positive current $+I_S$, while a logic 0 is transmitted as a negative current $-I_S$. An internal termination resistor converts this current to a differential voltage, which is being sensed by a differential amplifier. For the implementation in this thesis, I_S is chosen to be 5mA, with the termination resistor chosen to be 50Ω . The voltage sensed across the differential amplifier is thus $\pm 125mV$.

A current mode signalling system has several advantages over a voltage level signalling system. First, with the use of current steering as shown in Figure 2-1, the current supply to the driver is always kept at I_S. The Ldi/dt noise added to the power supply planes is thus reduced. Moreover, given a differential amplifier with a reasonable common-mode signal rejection performance, the signal transmitted would

Figure 2-2: A Simultaneous Bidirectional Signalling System

have higher immunity to power supply noise. The sensing of a signal simply does not depend on a power plane.

A current mode system is more pin efficient than a traditional differential pair signalling system, although the latter may have comparable power supply noise rejection performance. A differential pair has a 2:1 pin to signal ratio, while a current mode system has a ratio closer to unity. This is because V_T, the power-supply-independent reference plane, of a current mode system can be shared among several signals.

2.2 Simultaneous Bidirectional Signalling

A current mode signalling system can be easily extended to a simultaneous bidirectional signalling system. Figure 2-2 shows a bidirectional signalling system.

In a bidirectional signalling system, a reference copy of the transmitted signal is produced locally for the differential amplifier. The amplifier can thus subtract this voltage off the voltage on the line and generate the received signal. This simple idea of super-position is further illustrated in Figure 2-3. In the diagram, signal 4 is the signal as seen on the left end of the signal line. The receiver on the left hand side subtracts the local signal 1 from signal 4 to generate the incoming signal, namely, signal 3.

The ratio k in Figure 2-2 is a number smaller than 1. This reduces the on-chip

Figure 2-3: Super-position of Bidirectional Signals

current and thus the power consumption. For the ease of sizing the transistors, k is chosen to be 0.2, i.e. a 5 times scale down of the original driver.

Chapter 3

Receiver Circuit

The small voltage swing of the transmitted signal at the receiver internal termination resistor could not be used directly for on-chip logic. A Chappell differential amplifier[2] is used to convert the received signal to standard logic levels. This chapter describes the design and the performance of the Chappell amplifier used in the simultaneous bidirectional driver.

3.1 Chappell Amplifier

The Chappell amplifier was originally designed for converting ECL signals to TTL signals. Figure 3-1 shows the circuit diagram of a Chappell amplifier sized for the 0.8μm process. Employed in the bidirectional driver, it converts a 125mV signal about a reference voltage to TTL logic level, which implies a required gain of 20.

The amplifier consists of three stages: a differential amplifier and two inverter restoring stages. Q2 and Q4 forms an ordinary differential pair. The high speed of the amplifier comes from the bias voltage variation at the gate of current source Q5. As an illustration: when IN goes up, more current drains down Q2 of the differential pair, which implies that the bias voltage of current source Q5 decreases. This reduces the current flowing down Q4 faster than a simple differential pair, which means OUT changes faster. The opposite happens when LINE goes down.

Figure 3-1: Receiver Circuit for a 0.8μm Process

3.2 Performance

3.2.1 Speed

The speed at which the amplifier operates is limited by its ability to resolve a single pulse from the incoming signal stream. A single up-going pulse and a single down-going pulse should have a small pattern sensitive skew when compared to level switching signals; this ensures that a clock could sample the correct signal regardless of the data stream pattern. The pulses should also have little distortion in pulse width when compared to the input signal; this ensures that the pulses are wide enough to be sampled.

The measurements in Figure 3-2 were done with input pulses centered at 2.5V with a 250mV peak-to-peak swing. The input pulses spend 40% of the pulse width in rise time and fall time. The pulse widths of the vairous isolated pulses were measured. The pattern sensitive skews of the pulses when compared to a level-switching signal are also measured.

The measurements indicate that the amplifier operates at a maximum of 660 MBits per second. Even at this high speed, the output pulses have less than 0.3ns in pattern sensitive skew and preserve at least 75% of the input pulse width. A simple

	Down-going		Up-going	
Input Pulse Width	t-width	t-skew	t-width	t-skew
2.5ns	2.21ns	-0.17ns	2.48ns	-0.28ns
2.0ns	1.76ns	-0.14ns	2.03ns	0.03ns
1.5ns	1.11ns	0.11ns	1.51ns	0.06ns
1.25ns	failed	failed	1.13ns	0.26ns

Figure 3-2: Amplifier Pulse Width and Distortion Measurements

latch is thus sufficient for sampling these pulses correctly.

Figure 3-3 shows the amplifier operating at 400 MBits per second, while figure 3-4 shows the amplifier operating at 660MBits per second. The latter also indicates that the down-going pulse starts rising before it can reach the rail.

A further examination at the inputs to the first inverter of the receiver, in figure 3-5, shows the limitations on the speed of the receiver. For a 660 MBits per second down-going pulse, the input voltage to the first inverter could not go as low as a steady logic 0 does. This implies that the gain of the first-stage differential amplifier is too large. To increase the speed of the receiver, the gain of the differential amplifier should be decreased and shared among the two inverter stages. The best performance would be obtained if the three stages of the amplifier have the same gain.

Figure 3-3: Signal Stream at 400 MBits Per Second

Figure 3-4: Signal Stream at 660 MBits Per Second

Figure 3-5: Input to the First Receiver Inverter at 660MBits Per Second

3.2.2 Power

The amplifier on a 0.8μm process consumes 14.8mW of power on a worst-case power HSPICE simulation. This power is mainly consumed by the 2.3mA current draining down the differential pair. An increase in this current implies an increase in g_m,[7] which means an increase in gain. The design described here, however, opts for a lower power consumption and employs a total of two inverters to achieve the required gain.

3.2.3 Common Mode Noise Rejection

HSPICE simulation indicates that for an input signal of 125mV above or below the reference voltage V_T, a valid DC range of V_T is 1.4V to 3.2V. Figure 3-6 shows further that the amplifier can operate at 400 MBits per second with the reference voltage varying with the input signal. The simulation result implies that for a V_T of 2.5V, the amplifier can totally reject an AC common mode signal with a frequency of 200MHz and a magnitude of 0.7V.

Figure 3-6: Test of Common Mode Noise for Chappell Amplifier

Chapter 4

Transmitter

This chapter describes the transmitter for the simultaneous bidirectional driver. The transmitter is made up of a pair of current sources, which sink either a positive or a negative current into the termination resistors of the signal line. To allow operation at high speed, the transmitter employs current steering to minimize the noise induced onto the power planes; it also makes use of a rise time control mechanism to reduce signal reflections on the signal line.

4.1 Steered Current Sources

Figure 4-1 shows the block diagram of the current mode transmitter. The transmitter sinks a current of either +5mA or -5mA into the termination resistors of the signal

Figure 4-1: A Current Mode Transmitter with Current Steering

Figure 4-2: A Steered Cascode Current Source

line, depending on the binary value of the signal. As the diagram indicates, the current drained from the power and ground planes always stays at 5mA, no matter which way the switches flip. This virtually eliminated the Ldi/dt noise induced onto the supplies planes.

Figure 4-2 shows a naive implementation of the transmitter circuit. It is basically a pair of cascode current sources, which is chosen because of their good power supply noise rejection property. The transistors are biased to remain in saturation. Figure 4-3 shows the biasing circuit sized for a 0.8μm process.

4.2 Rise-Time Control

The signal generated by the the transmitter in Figure 4-2, however, is noisy because of the chip package. As the transmitter is driving the signal line with fast edges, the switching noise caused by reflections could become so severe that the original signal could not be recovered. Studies have shown that the amplitude of signal reflections on chip packages increases with decreasing rise/fall time [1]. A simulation from [6] is repeated here to illustrate the effects of rise/fall time on reflection.

Figure 4-3: Biasing Circuit for a 0.8μm Process

Figure 4-4: A Simple Interconnect Model

Figure 4-5: Simulation for Rise Time Noise

Figure 4-4 shows a simple interconnect model for two inter-chip connection points[1]. The graphs in figure 4-5 correspond to input current applied to the model, with a 0.1ns and a 1ns fall time respectively. The graphs show that the signal has a smaller reflection and is less glitchy when it has a slower fall time. A rise/fall time control mechanism is thus employed for the simultaneous bidirectional driver to slow down the signal rise/fall time.

Figure 4-6 is the modified transmitter designed for the simultaneous bidirectional driver on a 0.8μm process. The inverter array staggers the turn-on for five equally-sized steered current sources, which together provide the required 5mA of current. Figure 4-7 shows the signal on a line as driven by a naive transmitter and an improved transmitter with staggered turn-on. The modified transmitter has cleaner edges than the original transmitter.

[1] Please refer to [4, 3] for information on simple chip interconnect models.

Figure 4-6: Transmitter with Staggered Turn-on for a 0.8μm Process

Figure 4-7: Comparison of Naive Transmitter with Improved Transmitter

Figure 4-8: Power Supply Noise Rejection for the Transmitter

4.3 Performance

4.3.1 Power Supply Noise Rejection

Figure 4-8 shows the results of the HSPICE AC analysis of power supply noise rejection. The figure indicates that the transmitter maintains a power supply rejection of below -20dB for frequencies below 200MHz. This ratio maintains below -10dB for frequencies up to 1GHz. The good power supply noise rejection performance comes from the cascode current source of the transmitter, which is chosen despite its large transistors.

4.3.2 Speed

The staggered transmitter in figure 4-6 has a rise/fall time of about 1ns, which is optimized for operation at 400MBits per second, i.e. a 2.5ns pulse width. As mentioned in section 4.2, rise/fall time control for the transmitter is required because of signal reflections on the chip interconnections. Indeed, HSPICE simulation has shown that a naive one-stage transmitter is capable of switching the required 5mA of current at a rate above 1GBits per second, given a perfect inter-chip connection as a simple transmission line. The limiting factor for the transmitter speed is thus the chip interconnections. The 1ns rise/fall time for our staggered transmitter is chosen to keep the signal reflections below 20 %, as indicated by figure 4-5 earlier in the chapter.

Chapter 5

Driver System

This chapter describes the design issues for integrating the different parts of the simultaneous bidirectional signalling system. It also provides a simple performance analysis for the system implemented on a 0.8μm CMOS process.

5.1 System Design

5.1.1 System Integration

The simultaneous bidirectional signalling system in figure 2-2 is assembled using the Chappell Amplifier as shown in figure 3-1, the biasing circuit as shown in 4-3, the transmitter circuit as shown in figure 4-6, and a feed-back circuit by sizing the cascode current sources in figure 4-6 5 times smaller.

5.1.2 Resistor Sizings

As shown in figure 2-2, given $Z_0 = 50\Omega$, the simultaneous bidirectional driver requires resistors of values 25Ω, 50Ω and 125Ω. These resistors are implemented as NMOS transistors biased in their linear region, i.e. input gates are connected to V_{dd}, so that $V_{gs} > V_{ds}$.

To compensate for process variation, a resistor sizing scheme from [10] is employed. The scheme adds three extra NMOS transistors in parallel with every required resistor.

Transistor Ratio	1X	2X	4X	8X	
% Variation in Ω	50Ω	100Ω	200Ω	400Ω	Effective Ω
$+20\%$	0	1	1	0	53.5Ω
$+10\%$	0	1	1	1	51.5Ω
-10%	1	0	0	1	48.9Ω
-20%	1	0	1	0	48.0Ω

Table 5.1: Resistor Sizings Compensation

Resistance (Ω)	Width (λ)	Length (λ)
25	320	2
50	160	2
100	80	2
125	64	2
200	40	2
250	32	2
400	20	2
500	16	2
1000	8	2

Table 5.2: Resistor Sizings for the HP 0.8μm Process

Process variation could be compensated by turning on the four parallel transistors' input gates in different combinations. [1] Table 5.1 shows the compensation scheme for a 50Ω resistor. The scheme is also implemented for the 25Ω and 125Ω resistors using the same transistor ratio as shown in the table. Table 5.2 shows the resistor sizings for the HP 0.8μm CMOS process.

5.2 System Performance

Figure 5-1 shows the simultaneous bidirectional signalling system being simulated in this section. The simple interconnect model is typical for modern chip packages.

Figure 5-2 shows the inputs and outputs when the drivers are running at 400MBits

[1] An automatic on-chip termination tuning FSM is proposed in [10]. Manual tuning is implemented here for the sake of simplicity.

Figure 5-1: Driver System

per second. The inputs signals are arranged so that all four combinations for the two inputs, i.e. 00, 01, 10 and 11, are tested. The simulation results shows that the design in this thesis is capable of doing simultaneous bidirectional signalling at 400MBits per second.

Figure 5-3 shows the superposition of the signals as seen at the two ends of the signal line. It also shows the feedback signals generated locally for the -ve inputs of the differential amplifiers, i.e. x7.feed and x8.feed. Because of noise caused by the chip interconnections, the differential signals at the two receivers do not always stay at the expected 125mV. The receivers, however, are capable of rejecting this noise and generating the correct logic output.

HSPICE simulation shows that the worst case power consumption for a pair of drivers is $75.1mW$. This implies that a single driver consumes $38mW$, which adds to about $4W$ for 100 drivers.

Figure 5-4 shows the current supplied to the V_T plane as the input signal switches. The diagram indicates that a maximum current of ±9mA is required for the the V_T plane for each pair of driver.

Figure 5-5 shows the current flowing through a V_T package pin at 400MBits per second. The digram indicates that the maximum rate of change of current is about 5mA/ns. Given a lead inductance of 3nH, we calculate that the Ldi/dt voltage induced inside the chip is about 15mV. For a receiver that can reject 50mV of differential mode noise, a V_T pin can thus be shared among 4 pairs of drivers, giving a pin-to-signal ratio of 1.25.

Figure 5-2: Inputs and Outputs of the Driver Running at 400MBits Per Second

Figure 5-3: Inputs to the Amplifiers at 400MBits Per Second

Figure 5-4: Current Supplied to the V_T Plane at 400MBits Per Second

Figure 5-5: Current Through A V_T Pin at 400MBits Per Second

Chapter 6

Implementation

This chapter describes a prototype chip which implements the simultaneous bidirectional driver on a 1.2μm process. [1] The chip includes logic for testing data integrity across the simultaneous bidirectional drivers.

6.1 Test Logic

Figure 6-1 shows the test logic block diagram for the prototype chip. The prototype chip includes both the logic for transmitting and receiving data; two identical chips are thus connected as a unit during testing.

The TRANSMIT logic puts onto the data line a 16-bit data half-word, appended with 4 bits of parity, on both edges of the transmit-clock. The 16-bit data half-word and the parity bits are selected by the transmit-clock through the "Half-word Select Mux". The 32-bit data word, on the other hand, can be selected from different sources by the "Input Select Mux". The input can either be the on-chip "Bit Pattern Generator" or some off-chip sources. Each of the 32 bits of the data word could also be held fixed at 1 or 0. The data word is selected through the "Input Select Shift Register" as a test setup procedure.

The RECEIVE logic simply checks the data parity data on both edges of the receive-clock. It asserts an error signal if a parity error is detected.

[1] The logic design and layout is done in collaboration with Larry Dennison of the MIT CVA group.

Figure 6-1: Test Logic Block Diagram

6.2 Fabrication

The prototype chip is fabricated using the HP 1.2μm process provided by MOSIS; it is then packaged in an 84-pin LCC ceramic chip carrier.

Although the original driver was designed for a 0.8μm process, a 1.2μm process is used because of the project submission deadline set by MOSIS. The original driver design remains the same except for the new resistor sizings as shown in table 6.1. HSPICE simulation shows that the simultaneous bidirectional driver behaves with little or no performance degradation on a 1.2μm process. This could be explained by the fact that the performance of the driver is limited by the chip interconnections.

Resistance (Ω)	Width (λ)	Length (λ)
25	380	2
50	190	2
100	96	2
125	76	2
200	48	2
250	38	2
400	24	2
500	20	2
1000	10	2

Table 6.1: Resistor Sizings for the HP 1.2μm Process

Chapter 7

Conclusion

This thesis described and analysed the design of a simultaneous bidirectional driver that allows point-to-point digital signalling at 400MBits per second in both directions, over the same pin, and at the same time. The driver doubles the interchip bandwidth of a chip package pin and allows digital design engineers to use simpler packaging technology as they put more logic onto a chip.

This thesis concludes that the limiting factor on the speed of the driver is the reflections and noise caused by the chip interconnections, instead of the performance of the devices.

Further studies can be done on optimizing the rise-time control mechanism of the transmitter circuit to allow operation at higher speed. Experiments could be set up to measure and model various high peformance packages [1] so that a more general rise-time control mechanism could be derived for accommodating different packages.

[1] Please refer to Appendix A for information on package models.

Appendix A

Package Model

Currently, most specifications for chip packages on the market do not include detailed AC characteristic information. Research has been conducted to collect chip package SPICE models from various vendors. The result is not satisfying, either because of their reluctance to release such models, or because that they do not have such information.

Some organizations, however, have begun to realize the importance of such models. MOSIS has purchased new instruments to characterize the packages supplied through them; Vitesse is actively hiring research scientists to work on modeling their packages; HP, which goes a step further, organizes periodic symposium to address the issue of high speed digital interconnections.

The rise-time simluation experiment in section 4.2 is repeated below for two package models obtained from vendors. They both showed input signals with fall times of 0.1ns and 1ns, and that the signal is less glitchy with a reduced fall-time.

Figure A-1 and A-2 show the model and the simluation result for a 250 pins INTEL PGA package. Figure A-3 and A-4 show that for a 344 pins LDCC package.

For research done on interconnections modeling, please refer to [13, 11, 12].

Figure A-1: Package Model for a 250 Pins INTEL PGA Package

Figure A-2: Simulation for Rise Time Noise on a 250 Pins INTEL PGA Package

Figure A-3: Package Model for a 344 Pins LDCC Package

Figure A-4: Simulation for Rise Time Noise on a 344 Pins LDCC Package

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