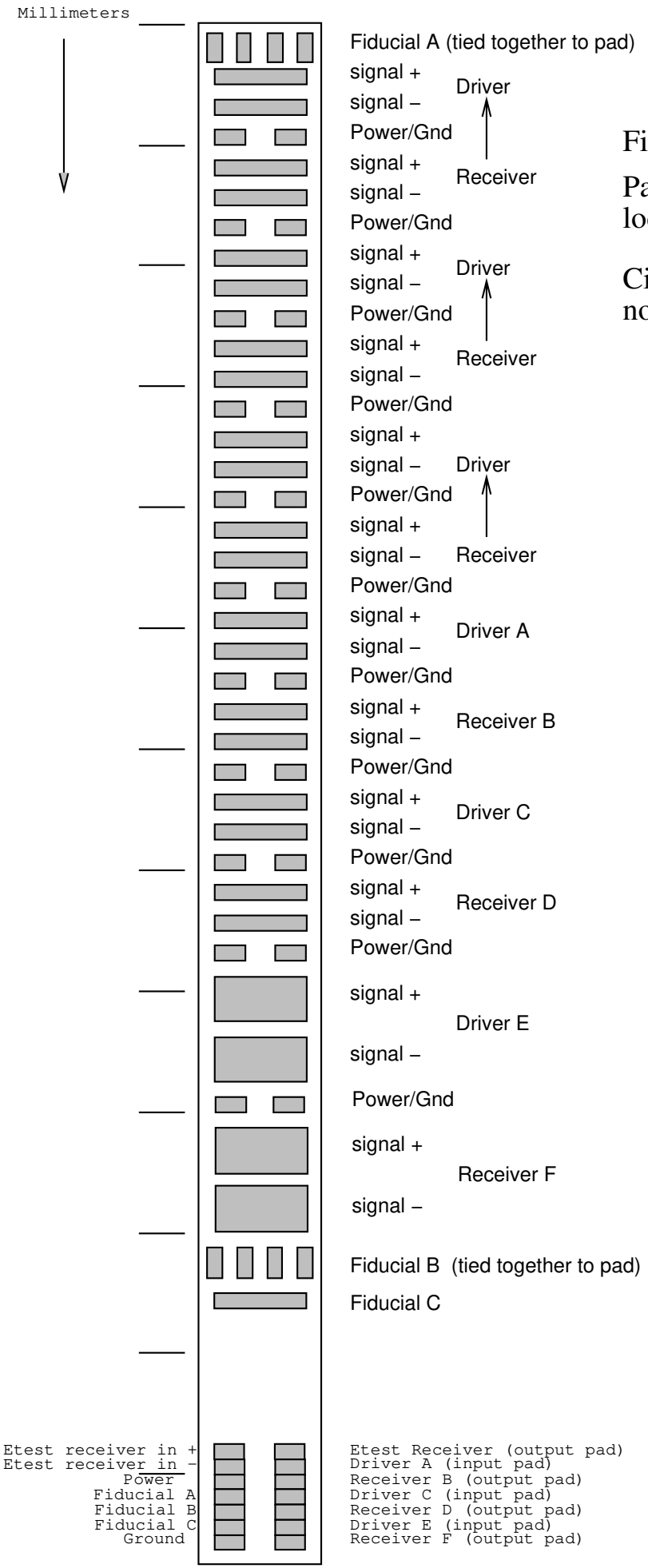
Physical Layout, Polychip test chip



Final Layout Size 1 mm x 12.76 mm

Pads shown are metal3 capacitive pads located on a 125 micron grid.

Circuitry should be located in areas not covered by metal3 capacitive pads