Massachvsetts Institvte of Technology

Department of Electrical Engineering and Computer Science

6.313 Contemporary Computer Design

Final has been scheduled for Monday Morning December 18 in Room 26-310/314

Problem Set #8 Fall, 1995, Due Wed 8 November

1. Intel was here yesterday talking about their future technology for constructing microprocessors, and gave the following comparison:

| Characteristic | Year 1995 | Year 2010 |
|---|---|---|
| Die size | 18 mm x 17 mm | 27 mm x 27 mm |
| Transistor count | 10 million | 1000 million |
| Feature size | 600 nm | 100 nm |
| Power supply voltage | 2.9 volts | 1.3 volts |
| Gate oxide thickness | 12 nm | 4 nm |
| Clock rate | 133 MHz | 4000 MHz |

What item has been left out of this chart which would give you pause as to the technological future of Intel's plans? Estimate a problematic number for how much worse things will be. Where would you invest your money as a research manager at Intel? What would the chart look like for the year 2020? Can you count on straight line extrapolation? What limits are approached? Hint: the P6 processor (aka "Pentium Pro") described above dissipates 20 watts.

2. A workstation box dissipates 200 watts of power, and requires forced air cooling. The box must operate in an ambient temperature range of 10 to 45 degrees C, and the maximum allowable air temperature within the box for reliable operation is 55 degrees. The specific heat of air is 0.249 calories/gram/degree, and the density of moist air at 50 C and 1 Bar is approximately 1.08 g/liter. Determine the minimum volume velocity of air required to remove the 200 watts of heat by forced convection.

3. You need to implement a fast 2048 bit shift register, and have a choice of available storage elements and clocking strategies. The basic gate delay is 100 ps. Fall time and rise times of typical logic signals are also 100 ps. You have determined that clock skew between different locations can be held to $\pm150$ pwith

careful wiring and clock distribution, but that clock skew between multiple clock phases, if used, cannot be controlled to better than $\pm 250$ ps.

a) Design a single phase clock waveform shape and single latch memory structure which will correctly implement the shift operation at maximum speed. What additional constraints must be obeyed in the single phase clock methodology, and what is the logic cost of such constraints?

b) Design a two phase non overlapping clock waveform pair and a latch pair memory structure which will correctly implement the shift operation at maximum speed. What constraints exist now? How does the speed and logic complexity compare?

c) Design an edge triggered clock waveform and D flip flop memory structure which will correctly implement the shift operation at maximum speed. What additional constraints must be obeyed in the single phase clock methodology, and what is the logic cost of such constraints? How does the speed and logic complexity compare?

4. A combinational logic circuit with a maximum total delay of 3 ns can be cleanly split into two pieces, one with a maximum delay of 1 ns and another with a maximum delay of 2 ns. You wish to clock these two pieces with an Earle latch structure, combining the latch into the last stage of logic in each portion. You want to use two latches to eliminate the constraint problems associated with single phase clocking. What additional information do I need to know before I am able to design the latch control signals (clock waveforms) for this structure? In particular, am I guaranteed that this circuit will function correctly if the two clock phases consist of waveforms with a period of 3 ns and an active time of 1.5 ns?